6.5V to 60V Input, Ultra-Low IQ, Integrated High-Side MOSFET, 3A/5A Buck DC/DC Converter with 3.3V/50mA LDO

1. Descriptions

The MK9163/5 operates over a wide input voltage range from 6.5V to 60V. With integrated the main MOSFET, delivers up to 3A/5A output current.

The MK9163/5 adopts a constant on-time (COT) control architecture to achieve excellent transient response.

MK9163/5 integrated a 3.3V fixed output LDO, which could deliver up to 50mA output current.

With patented standby circuits, the device can achieve ultra-low IQ, and exit the standby mode fast.

MK9163/5 supports pre-biased startup and integrated a boot refresh logic at every startup.

2. Applications

- GPS Tracker
- Automotive and Industry Systems
- Motor Drives, Telecom
- BMS

3. Features

- Wide Input Voltage 6.5V-60V
- Wide Output Voltage 1.22V-26V
- Integrated 72mΩ High-Side MOSFET
- Adjustable F_{SW} up to 500kHz
- <20μA Quiescent Current
- Internal 3.5ms Soft-start
- Smart Power Saving and Ultra-Fast Transient Response
- Precision ±1% Feedback Reference
- Integrated 3.3V/50 mA LDO
- OC, OT Protection with Hiccup Mode
- No Loop Compensation Components
- ESOP-8 Package with Thermal PAD

4. Typical Application

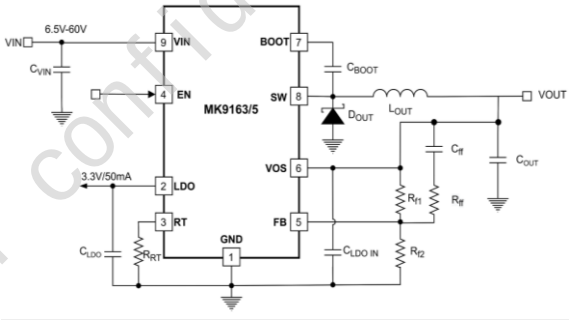


Figure 1. Typical Application Diagram

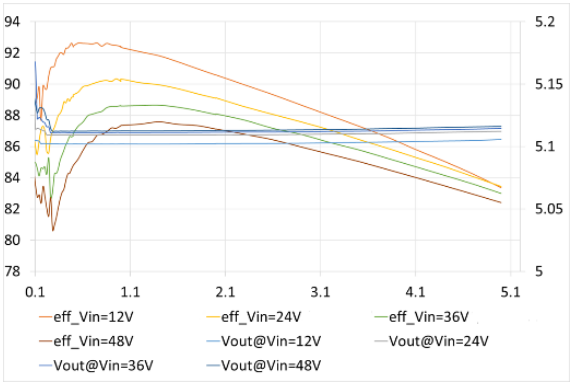
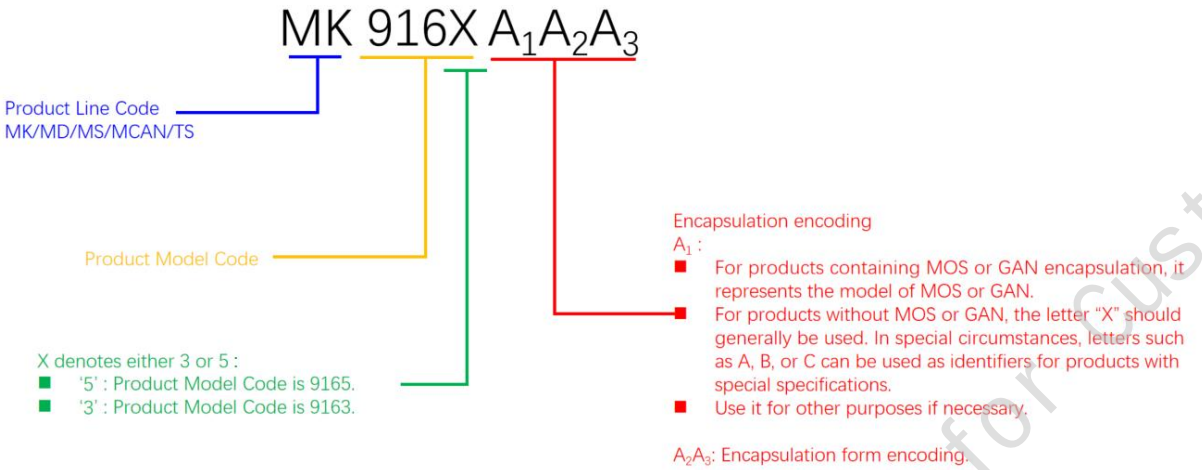


Figure 2. Efficiency and Load Regulation at 5V Vout

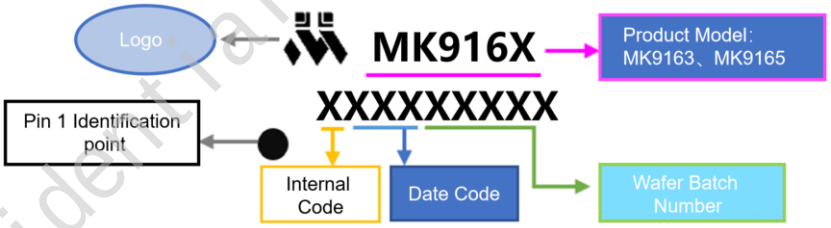
5. Order Information



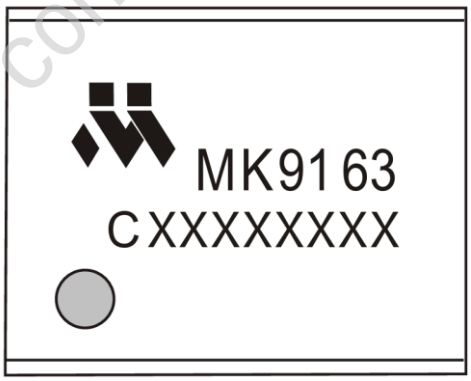
Part Number	Package Type	Package Qty	Eco Plan	MSL	Single Chip Weight	Output Current
MK9163CAD	ESOP8	4k/reel	RoHS & Green	3	70mg	3A
MK9165CAD	ESOP8	4k/reel	RoHS & Green	3	70mg	5A

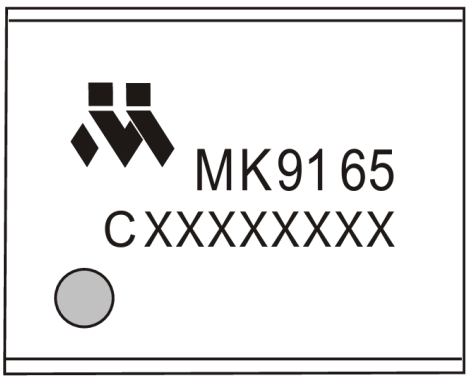
6. Pin Configuration and Marking Information

SOP/ESOP/ETSSOP/DFN/QFN



(Please refer to MRX-DM-SCM-04 for detailed rules)





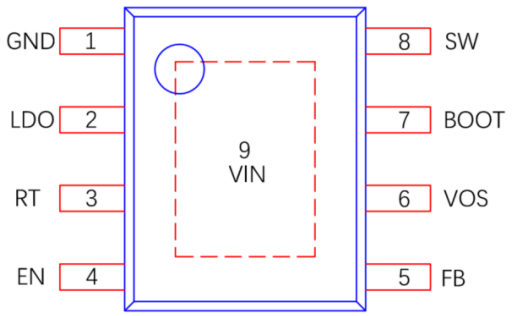


Figure 3 . Pin Function (top view)

Table 1. Pin Functions

Pin		I/O	Description
NO.	Name		
1	GND	Analog Input	Ground
2	LDO	Analog Power Output	3.3V LDO output, connect a capacitor to GND higher than 1uF; leave as float before device enabled to disable internal LDO.
3	RT	Analog Input	Connect a resistor to GND, set the switching frequency.
4	EN	Analog input	Buck and LDO enable, internal pull down by 0.08uA. Source 2uA after device enabled. Connect to VIN pin if hysteresis function is not used.
5	FB	Analog Input	Feedback input, connect to output voltage resistor divider.
6	VOS	Analog Power Input	Output sense and internal LDO input, connect to output cap with 100mA current capability PCB trace; Place 0.1uF cap close to VOS pin.
7	BOOT	Analog Power Input	Boot-strap pin. Decouple this pin to SW pin with a >100nF (0.2V drop) ceramic capacitor.
8	SW	Analog Power Output	Connect to the switch node of the power inductor and a schottky diode between this pin and GND.
9	VIN	Analog Power Input	Input pin. Decouple this pin to GND with low ESR capacitor. Connect to a VIN power plane to improve thermal performance.

7. Specifications

7.1 Absolute Maximum Ratings

		MIN.	MAX.	Units
Input voltages	VIN, EN, SW to GND	-0.3	60	V
	SW to GND (20ns pulse)	-3	60	
	BOOT to GND	-0.3	67	
	FB, RT to GND	-0.3	6.6	
	VOS to GND	-0.3	26	
Continuous drain current (2), TC=25 ℃	I_D	10		A
Pulsed drain current (3), TC=25 ℃	$I_{D, pulse}$	30		
Internal MOSFET breakdown voltage	BVDSS	60		V
Operating Junction Temperature, T_J		-40	125	℃
Storage Temperature, T_{stg}		-65	160	
Soldering Temperature (10 second), T_{sld}			260	

Notes:

(1) Stresses beyond the "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated in "RECOMMENED OPERATING CONDITIONS". Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Calculated continuous current based on maximum allowable junction temperature.

(3) Repetitive rating; pulse width limited by max. junction temperature.

7.2 ESD Ratings

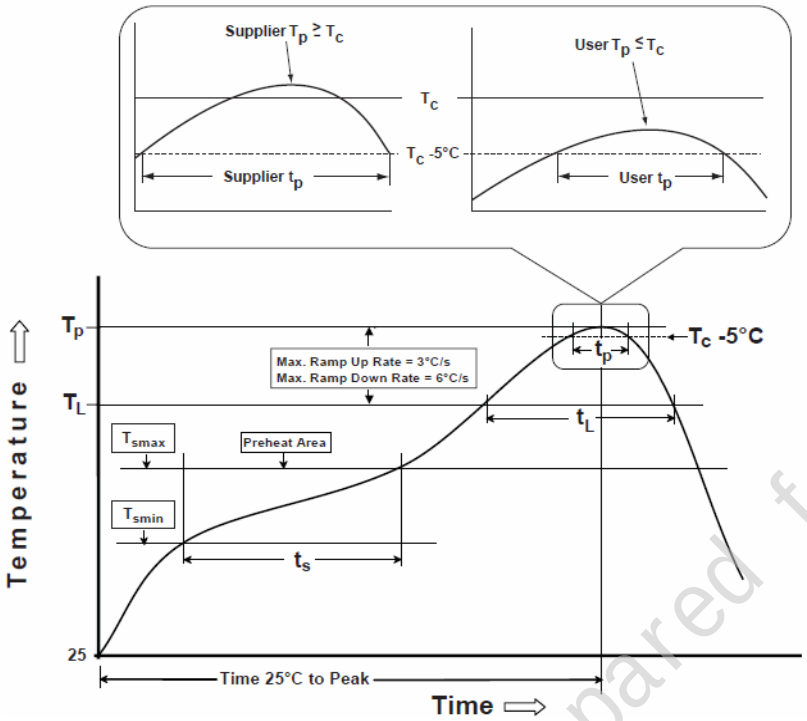
		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

7.3 Recommended Reflow Profile



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 100 ℃ 150 ℃ 60-120 seconds	 150 ℃ 200 ℃ 60-120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature (T_L) Time (t_L)maintained above T_L	183 ℃ 60-150 seconds	217 ℃ 60-150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the classification temp in Table2. For suppliers T_P must equal or exceed the classification temp in Table2	For users T_P must not exceed the classification temp in Table3. For suppliers T_P must equal or exceed the classification temp in Table3
Time (t_P) within 5℃ of the specified classification temperature (T_C)	20 seconds	30 seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8 minutes max
*Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum		

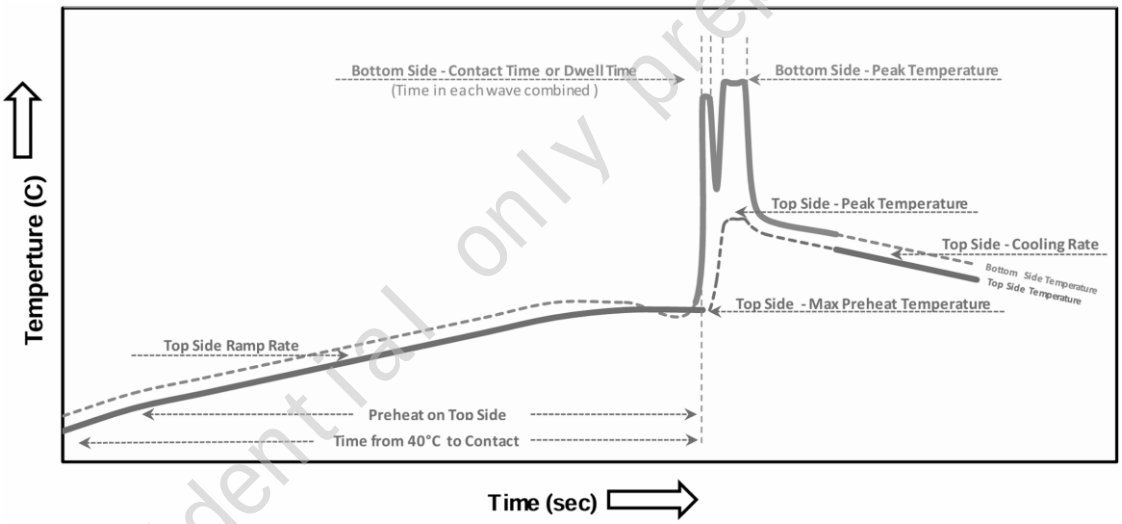
Table 1. SnPb Eutectic Process-Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5 mm	235 ℃	220 ℃
≥2.5 mm	220 ℃	220 ℃

Table 2. Pb-Free Process-Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6 mm	260℃	260℃	260℃
1.6 mm-2.5 mm	260℃	250℃	245℃
>2.5 mm	250℃	245℃	245℃

7.4 Recommended Wave Soldering Profile



7.5 Recommended Hand Soldering and Desoldering Methods

Hand Soldering

Selection of soldering iron	Flux	Iron temperature	Welding time
Sharp tip or cutting head	Use rosin type or non-cleaning flux (with a small amount of auxiliary wetting)	Sn Pb solder: 300-350℃ Lead free solder: 350-400℃	2-4 seconds per solder joint (to avoid overheating and damaging components or PCBs)

skill and notes:

(1) Heat the solder pad first, then send the solder wire.

(2) Avoid forcefully pressing the soldering iron tip.

(3) Pay attention to hand soldering ESD.

Hand Desoldering

Selection of desoldering tool	Use solder suction cups and soldering irons	Use hot air gun	Skill and notes
Solder sucker and soldering iron or Hot air gun	Iron temperature: Sn Pb solder: 300-350℃; Lead free solder: 350-400℃; Operation: Quickly heat the solder joint and then tin suction	Temperature: 300℃-400℃ Airflow: medium to low (to avoid blowing small components off). Time:≤10 seconds/solder joint. Preheating plate: 150℃-180℃ (bottom heating). Hot air nozzle: 250℃-300℃ (top heating).	(1). Clean the residual solder flux on the solder pads after desoldering. (2). Multilayer boards should be carefully avoided to prevent Pad detachment.

7.6 Recommended Operating Conditions

		MIN.	MAX.	Units
Recommended Operation Conditions	VIN Voltage	6.5	60	V
	EN Voltage	-0.3	60	
	SW Voltage	-0.3	60	
	Ambient Temperature	-40	+125	℃

7.7 Thermal Information

		Value	Units
Package Thermal Resistance	θ_{JA} (Junction to ambient)	30	℃/W
	θ_{JC} (Junction to case)	10	℃/W

7.8 Electrical Characteristics

V_{IN}=48V, V_{OUT}=12V, L=47μH, C_{OUT}=22μF, Typical values correspond to T_J=25℃, Minimum and Maximum limits apply over the full junction temperature range (-40℃ to 125℃) unless otherwise indicated.

Parameter		Test Conditions	MIN	TYP	MAX	Units
Input Voltage						
V_{IN}	Input Voltage		6.5		60	V
$V_{IN-UVLO}$	Input UVLO Off			5.65	6.3	V
$V_{IN-UVLO\_HYS}$	Input UVLO hysteresis			0.6		V
Supply Current						
$I_{SHUTDOWN}$	Shutdown Current	V_{EN}=0V		14	30	μA
I_Q	None switching quiet current	EN=V_{IN}, VOS higher than target, I_{LDO}=0A.		13		μA
$I_{STANDBY}$(1)	Standby Current	Reference design 2 Vin@48V, EN is pulled high from the outside.		35		μA
Feedback						
V_{REF}	Feedback reference voltage		1.2	1.22	1.24	V
EN						
V_{ENH}	EN rising threshold	V_{IN}=48V, I_{OUT}=0.1A		1.22	1.26	V
V_{ENL}	EN falling threshold		1.16	1.2		V
$I_{EN-Hysteresis}$	Hysteresis Input Current			-2		μA
Frequency (1)						
F_{SW}	Programmable Switching Frequency Range	Fsw(kHz)= $\frac{22\times10^3}{RT(k\Omega)}$			500	kHz
LDO						
V_{LDO}	LDO output voltage	VOS=12V, 0mA - 50mA	3.2	3.3	3.4	V
I_{LDOOC}	LDO over current	V_{LDO}=0V		55		mA
Timing						
t_{ON-MIN}	Minimum on-time			200		ns
$t_{OFF-MIN}$ (1)	Minimum off-time			200		ns
Power Switches						
$R_{DSON-HS}$	MK9165/MK9163	High-side MOSFET RDSON, TA=25℃		72		mΩ
Current Limit						

$I_{PEAK-HS}$	MK9163	High-side MOSFET Peak Current limit		5		A
	MK9165			7.5		
Soft Start						
t_{SS}	Soft-start time	V_{FB} from 0V to V_{REF}		3.5		ms
t_{Hiccup}	UVP Hiccup time (1)			60		ms
Under Voltage Protection						
V_{UVPF}	UVP Falling threshold	V_{FB} voltage		0.60		V
V_{UVPR}	UVP Rising threshold			0.62		V
Thermal Shutdown (1)						
T_{SD}	Thermal Shutdown Threshold	T_J rising		150		℃
T_{HYS}	Thermal Shutdown Hysteresis			20		℃

Note:

(1) Values are verified by characterization on bench, not tested in production.

7.9 Typical Characteristics

V_{IN}=48V, V_{OUT}=12V, L=47μH, C_{OUT}=22μF, T_A=25℃, unless otherwise specified.

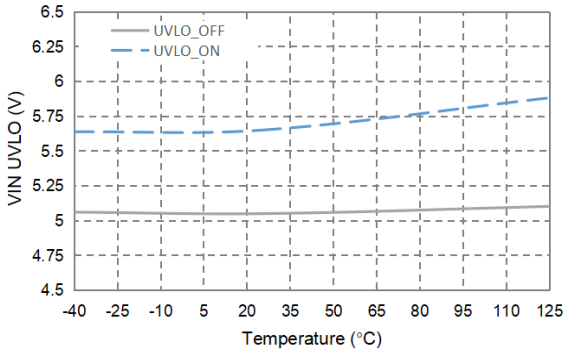


Figure 4. VIN UVLO v.s. Temperature

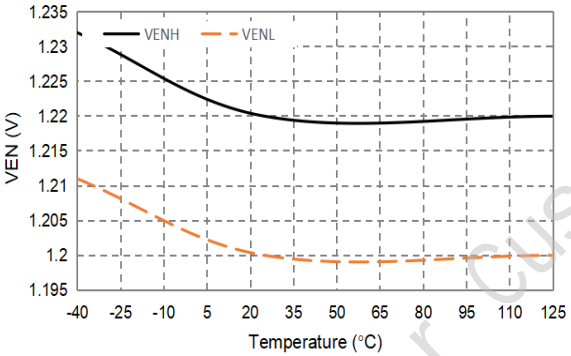


Figure 5. VEN v.s. Temperature

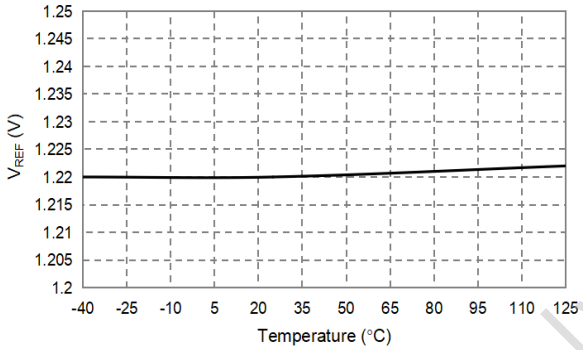


Figure 6. V_{REF} v.s. Temperature

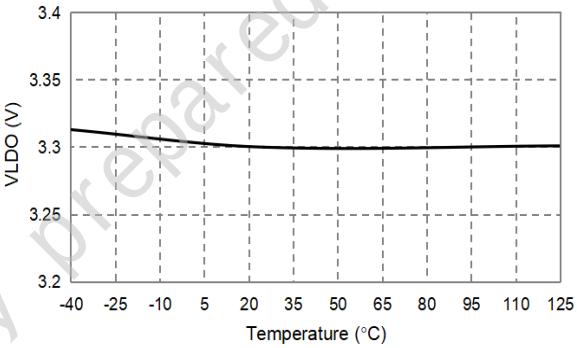


Figure 7. V_{LDO} v.s. Temperature

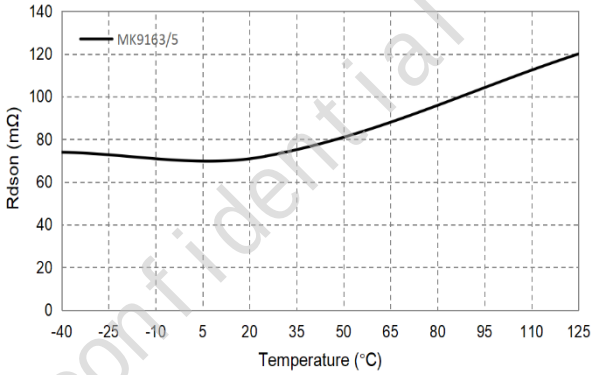


Figure 8. Rdson v.s. Temperature

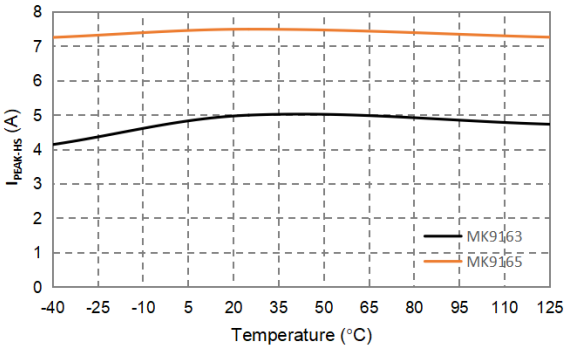


Figure 9. $I_{PEAK-HS}$ v.s. Temperature

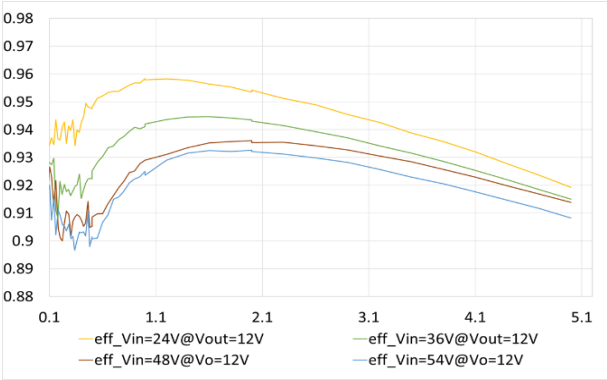


Figure 10. Efficiency at 12Vout

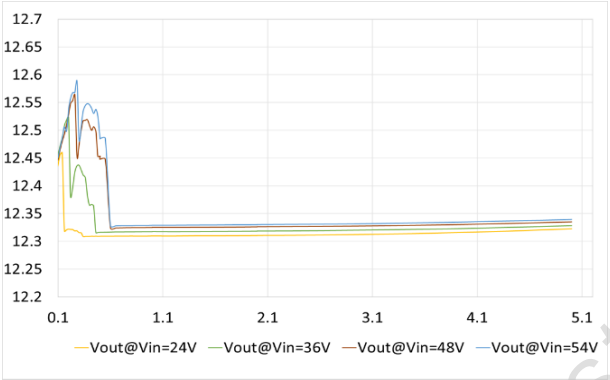


Figure 11. Load and Line Regulation at 12Vout

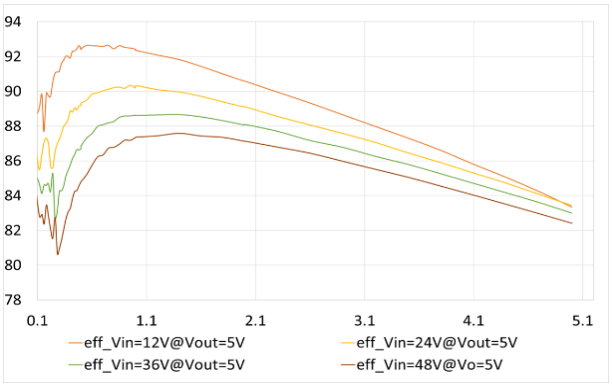


Figure 12. Efficiency at 5Vout

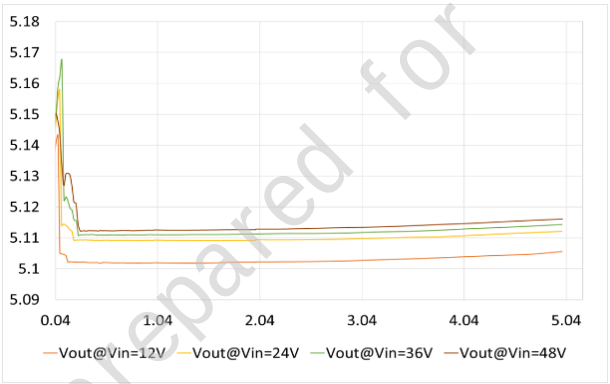
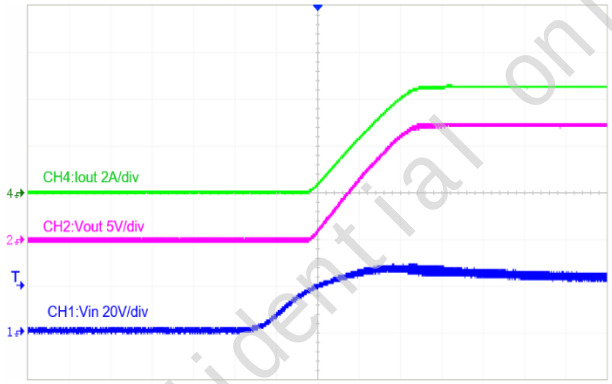
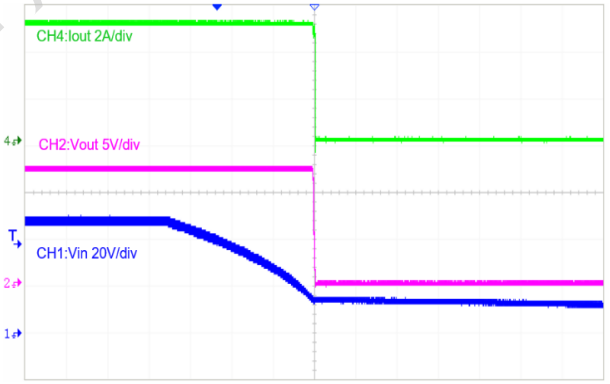


Figure 13. Load and Line Regulation at 5Vout



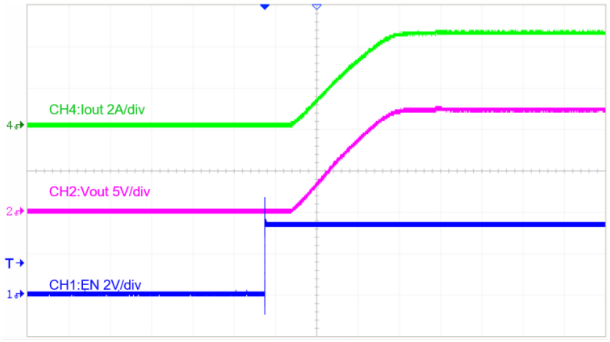
Time(1ms/div)

Figure 14. Startup from VIN



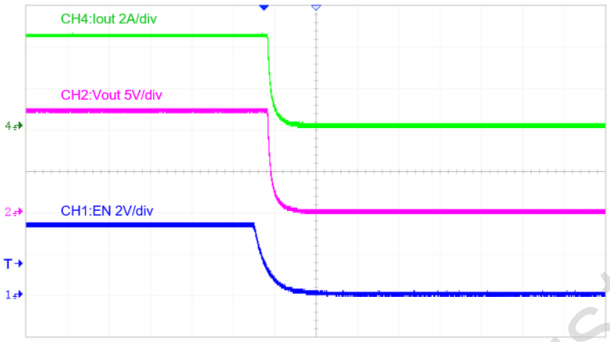
Time(5ms/div)

Figure 15. Shutdown from VIN



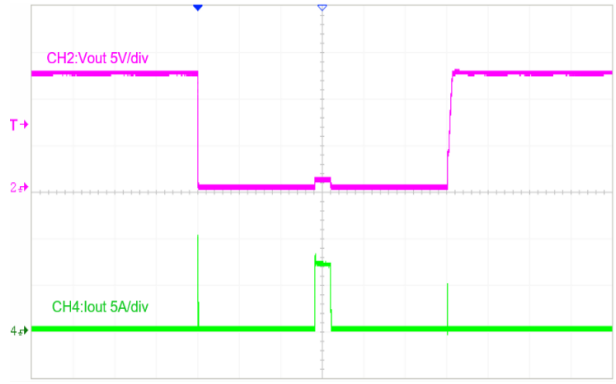
V_{IN}=48V Time(1ms/div)

Figure 16. Startup from EN



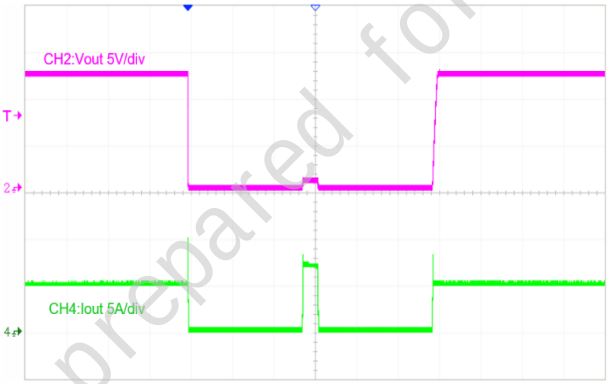
V_{IN}=48V Time(1ms/div)

Figure 17. Shutdown from EN



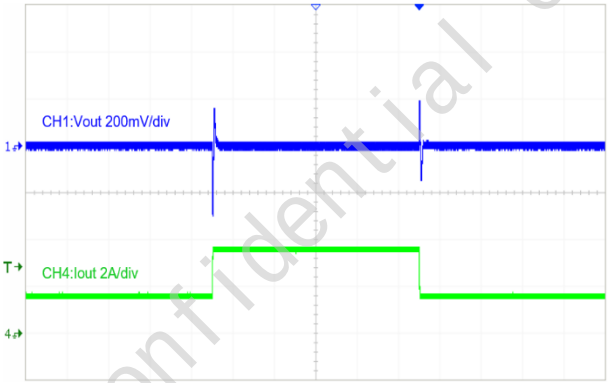
V_{IN}=48V I_{OUT}=0A Time(20ms/div)

Figure 12. Short Protection and Recovery



V_{IN}=48V I_{OUT}=3A Time(20ms/div)

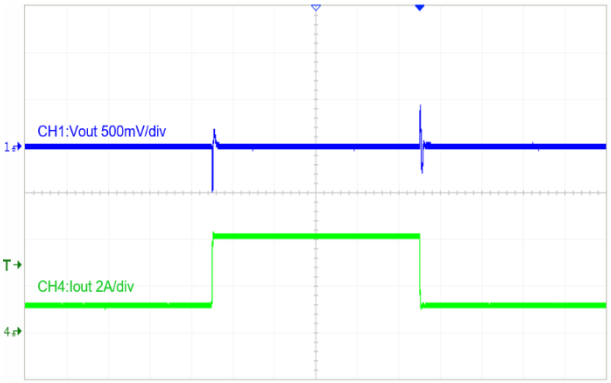
Figure 19. Short Protection and Recovery



V_{IN}=48V V_{OUT}=5V Time(1ms/div)

I_{OUT}:1.5A ~ 3.5A,3A/us

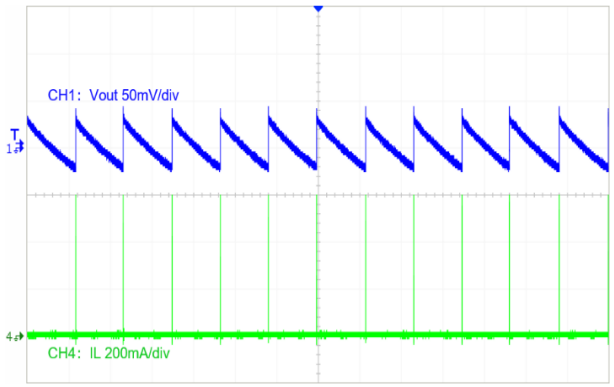
Figure 20. Load Transient



V_{IN}=48V V_{OUT}=5V Time(1ms/div)

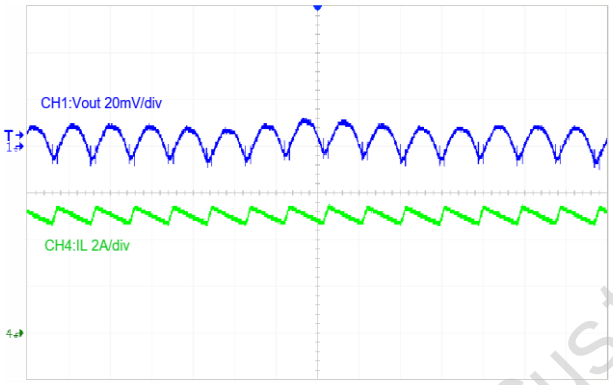
I_{OUT}:1A ~ 4A,3A/us

Figure 13. Load Transient



V_{IN}=48V V_{OUT}=5V Time(20ms/div) I_{OUT}=0A

Figure 22. Out Ripple



V_{IN}=48V V_{OUT}=5V Time(5μs/div) I_{OUT}=3A

Figure 23. Out Ripple

8. Detailed Description

8.1 Overview

The MK9163/5 operates over a wide input voltage range from 6.5V to 60V. With integrated the main MOSFET, the MK9163/5 delivers up to 3A/5A output current. The MK9163/5 adopts a constant on-time (COT) control architecture to achieve excellent transient response. MK9163/5 integrates a fixed output LDO, which can deliver up to 50mA output current. With patented standby circuits, the device can achieve ultra-low IQ, and exit the standby mode fast.

8.2 Functional Block Diagram

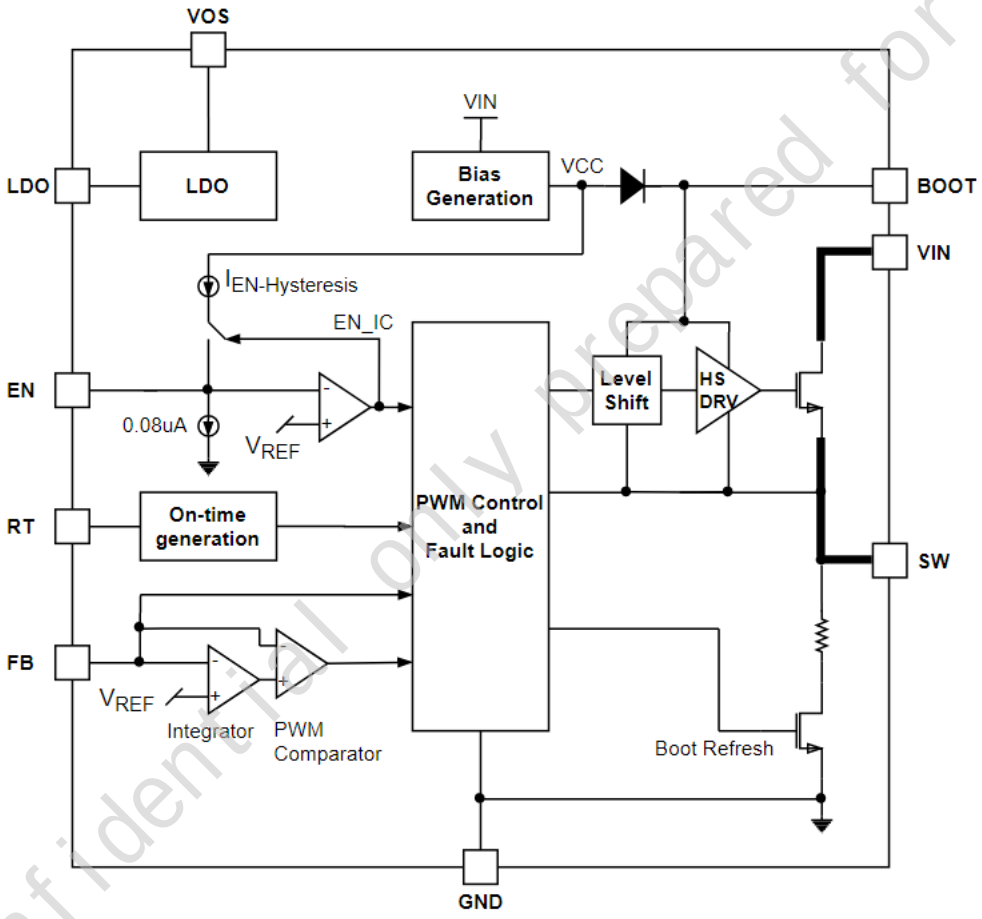


Figure 24. Block Diagram

8.3 Feature Description

8.3.1 Switching Frequency (RT)

The switching frequency of MK9163/5 is set by the on-time resistor RT. As shown in 5, a 110kΩ resistor sets the switching frequency at 200kHz.

$$F_{SW}(kHz) = \frac{22 \times 10^3}{RT(k\Omega)}$$

Note that the final switching frequency is affected not only by component tolerance but also by $t_{ON\text{-}MIN}$ and $t_{OFF\text{-}MIN}$.

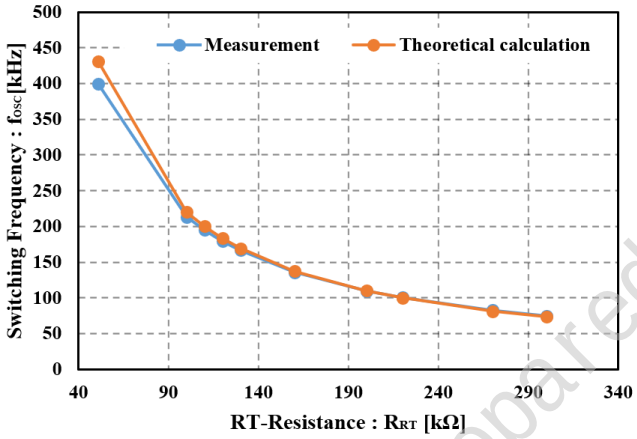


Figure 25. Switching Frequency v.s. RT-Resistance

8.3.2 Output Voltage Program

Choose R_{f1} and R_{f2} to program the output voltage. For target V_{OUT} setpoint, calculate R_{f1} and R_{f2} using below equation:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_{f1}}{R_{f2}})$$

V_{REF} is Feedback reference voltage, typical is 1.22V.

R_{f1} in the range of 100kΩ to 500kΩ is recommended for most applications. Larger feedback resistors consume less DC current, which is important if light-load efficiency is critical. But too large of resistors are not recommended as the feedback path would become more susceptible.

The feedforward capacitor C_{ff} and feedforward resistor R_{ff} are strongly recommended, which can improve the system stability and transient responses.

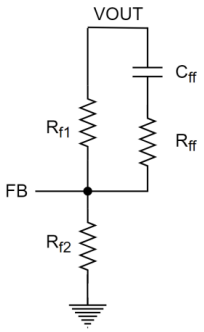


Figure 26. Feedback Resistance

8.3.3 Input Capacitor (CIN)

An input capacitor is necessary to limit the input ripple voltage while providing AC current to the buck converter at every switching cycle. The input ripple voltage ΔV_{IN} at input capacitor is calculated as:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} \geq \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})}$$

To minimize the potential noise problem, a X5R or better grade capacitor with sufficient voltage rating is recommended. This capacitor should be close to the VIN and GND pins to minimize the loop area formed by C_{IN} and VIN/GND pins. In this application, a 1μF low ESR ceramic capacitor is recommended.

8.3.4 Output Inductor (L)

It is recommended to choose the ripple current of inductor between 30% to 50% of the rated load current I_{OUT}(max) for most applications. The inductance is calculated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

And the peak current of inductor is calculated as:

$$I_L(\text{peak}) = I_{OUT}(max) + \frac{\Delta I_L}{2}$$

The saturation current rating of the inductor must greater than the I_L(peak). An inductor whose saturation current is above the current limit setting of the MK9163/5 will be the best choice. Note that inductor saturation current levels generally decrease as the inductor temperature increase.

8.3.5 Output Capacitor (COUT)

The output capacitor limits the capacitive voltage ripple at the converter output. This voltage ripple which is generated from the triangular inductor current ripple flowing into and out of the capacitor can be calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times F_{SW} \times C_{OUT}}$$

Above equation only takes the steady state ripple into consideration. The transient requirements also must be taken into consideration when selecting the output capacitor. The X5R or better grade ceramic capacitor larger than 22μF is recommended. For high peak current applications, an E-cap larger than 100uF is recommended too.

8.3.6 Enable Operation

Input UVLO can be programmed by EN rising threshold. The UVLO turn-on voltage can be calculated as:

$$V_{UVLO} = (1 + \frac{R_{EN1}}{R_{EN2}}) \times V_{ENH}$$

V_{ENH} is EN rising threshold voltage, typical is 1.22V.

The UVLO hysteresis is accomplished with an internal current source, $I_{EN\_Hysteresis}$ (typical is 2μA). When EN High the current source is connected with resistor divider and it is activated to quickly raise the voltage at the EN pin. The UVLO hysteresis can be calculated as:

$$V_{hys}(\mathrm{V}) = R_{EN1} \times I_{EN\_Hysteresis} + V_{EN\_HSY} \times \left(1 + \frac{R_{EN1}}{R_{EN2}}\right)$$

V_{EN_HSY} is EN threshold voltage hysteresis, $V_{EN\_HSY} = V_{ENH} - V_{ENL}$.

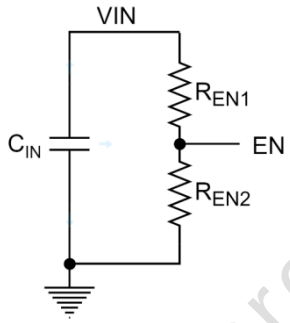


Figure 27. Enable Resistance Divider

Tie EN pin to VIN if hysteresis function is not used to improve quiescent current.

8.3.7 Boot-strap capacitor

This capacitor provides the energy for the high-side gate driver. A high quality 100nF ceramic capacitor connected between the BS pin and the SW pin is recommended. Also a RC series net can be used to slow down the turn-on speed of high side MOSFET.

8.3.8 Catch diode

MK9163/5 should be taken to connect external catch diode between the SW pin and the GND pin. The diode should comply with absolute maximum ratings of application. Opposite direction voltage should be higher than maximum voltage of the VIN pin. Also for saturation current of diode, select the one with larger current than the total of maximum output current and 1/2 of inductor ripple current ΔIL. Choose catch diode with lower voltage drop to enhance efficiency and thermal performance, for example V15PM6HM3/H from Vishay.

8.3.9 LDO

MK9163/5 integrates a 3.3V/50mA LDO, which is suitable for MCU's bias input. The LDO converters VOS to 3.3V with 50mA capability, with a ceramic cap >1μF as close as possible to LDO pin in application.

9. Application and Implementation

9.1 Reference design 1

Parameter	Symbol	Specification Value
Input Voltage	VIN	24V ~ 60V
Output Voltage	VOUT	5.1V
Switching Frequency	F_{SW}	200kHz (Typ.)
Maximum Output Current	$IOUT_{MAX}$	5A

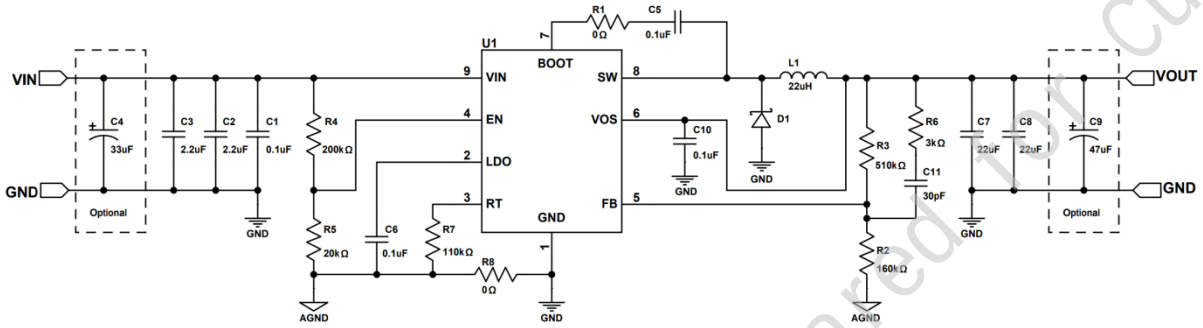


Figure 28. VOUT=5.1V Schematic

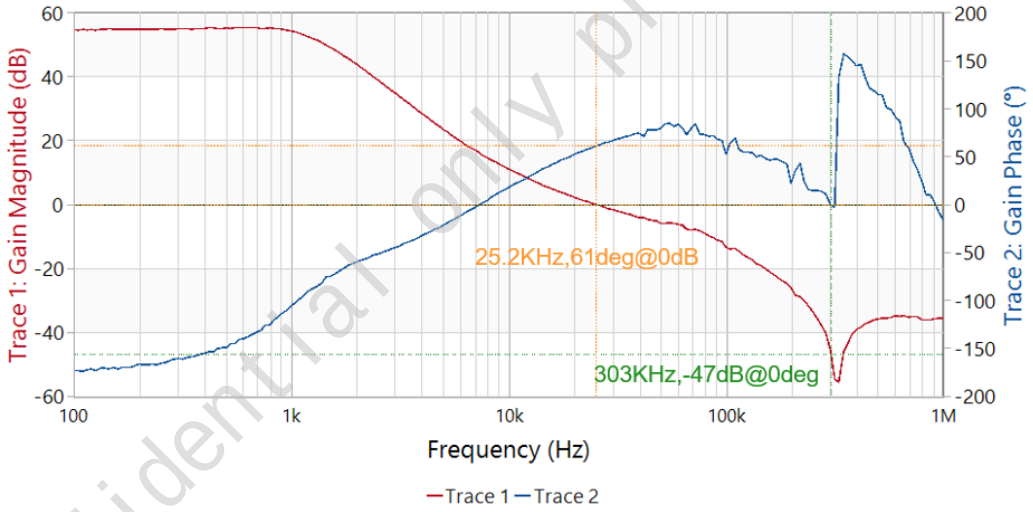


Figure 29. Frequency Characteristics (IOUT = 5.0A, VOUT=5.1V)

9.2 Reference design 2

Parameter	Symbol	Specification Value
Input Voltage	VIN	24V~ 60V
Output Voltage	VOUT	12.3V
Switching Frequency	F_{SW}	200kHz (Typ.)
Maximum Output Current	$IOUT_{MAX}$	5A

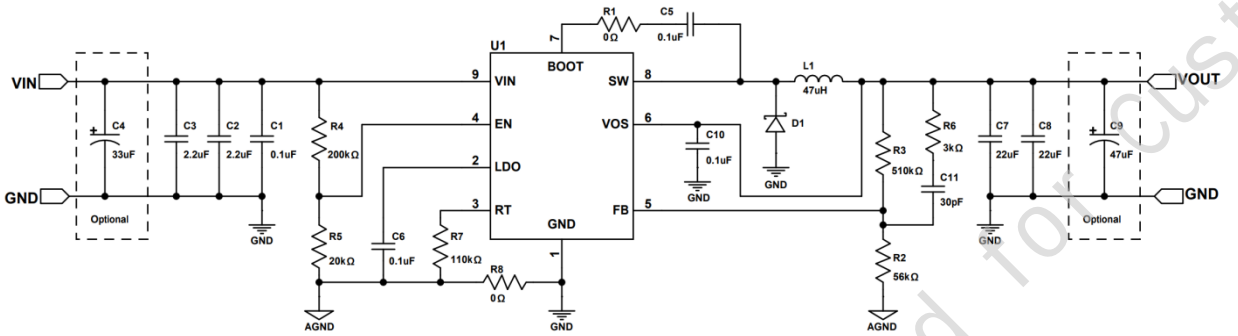


Figure 30. VOUT=12.3V Schematic

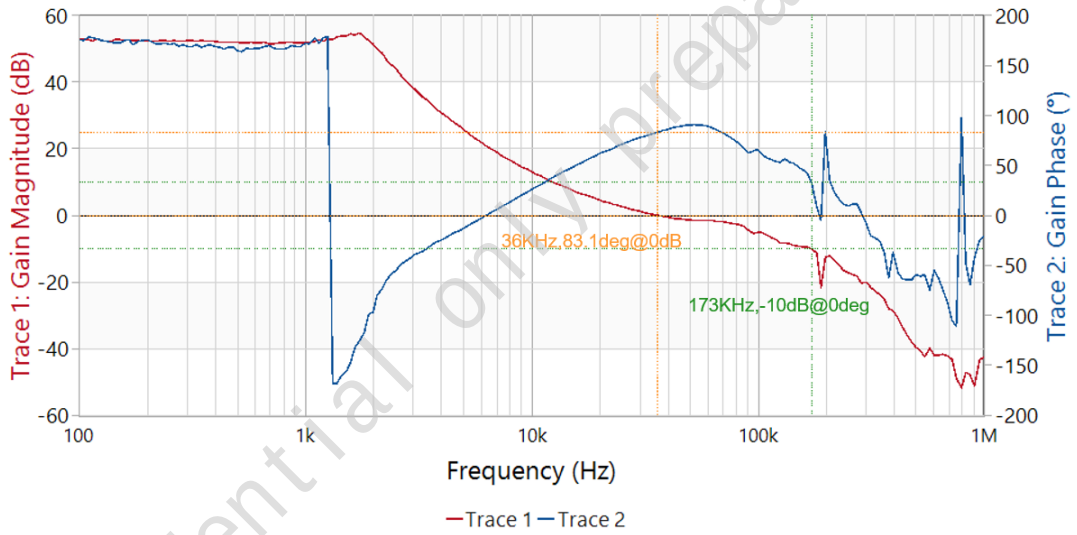


Figure 31. Frequency Characteristics (IOUT = 5.0A, VOUT=12.3V)

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9.3 Reference design 3

Parameter	Symbol	Specification Value
Input Voltage	VIN	35V~ 60V
Output Voltage	VOUT	24.3V
Switching Frequency	fosc	200kHz (Typ.)
Maximum Output Current	IOUTMAX	5A

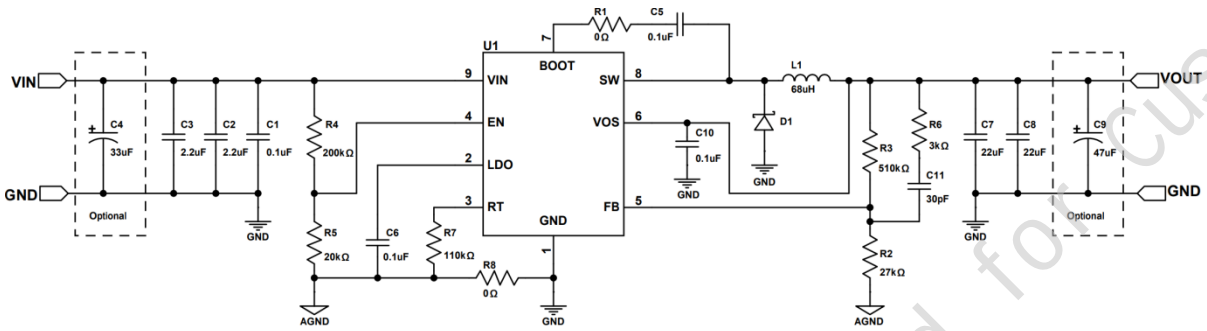


Figure 32. VOUT=24.3V Schematic

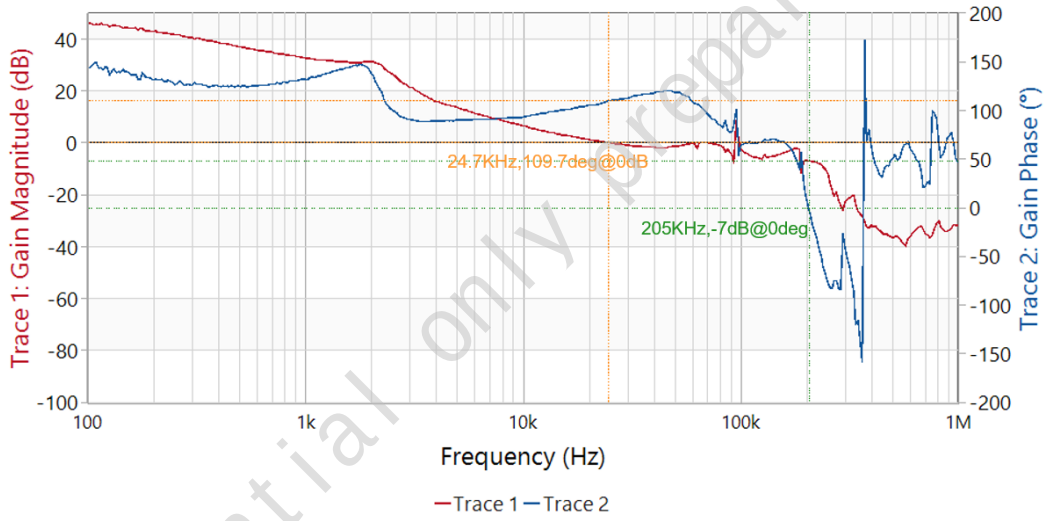


Figure 33. Frequency Characteristics (IOUT = 5.0 A, VOUT=24.3V)

10. Power Supply Recommendations

11. Layout

11.1 Layout Guidelines

To achieve high performance of the MK9163/5, the following layout tips must be followed.

(1) At least one low-ESR ceramic bypass capacitor CIN must be used. Place the CIN as close as possible to the MK9163/5 VIN and GND pins, place decoupling caps as close as possible between VIN and catch diode's GND.

(2) Minimize the loop area formed by CIN connections to VIN and GND pins.

(3) Inductor must be placed close to the SW pin. Minimize the area of SW trace to avoid the potential noise problem.

(4) Maximize the PCB area connecting to the VIN pin/thermal pad. If it is allowed, a ground plane can be used as noise shielding and heat dissipation path.

(5) Place the feedback resistors, R_{f1} and R_{f2}, close to the FB pin. Route the feedback VOUT sense path away from noisy nodes such as the SW net.

(6) Connect VOS pin to output cap directly, place a 0.1uF cap between VOS and GND.

(7) The RT pin is sensitive to noise. The on-time set resistor RT must be close to the device.

11.2 Layout Example

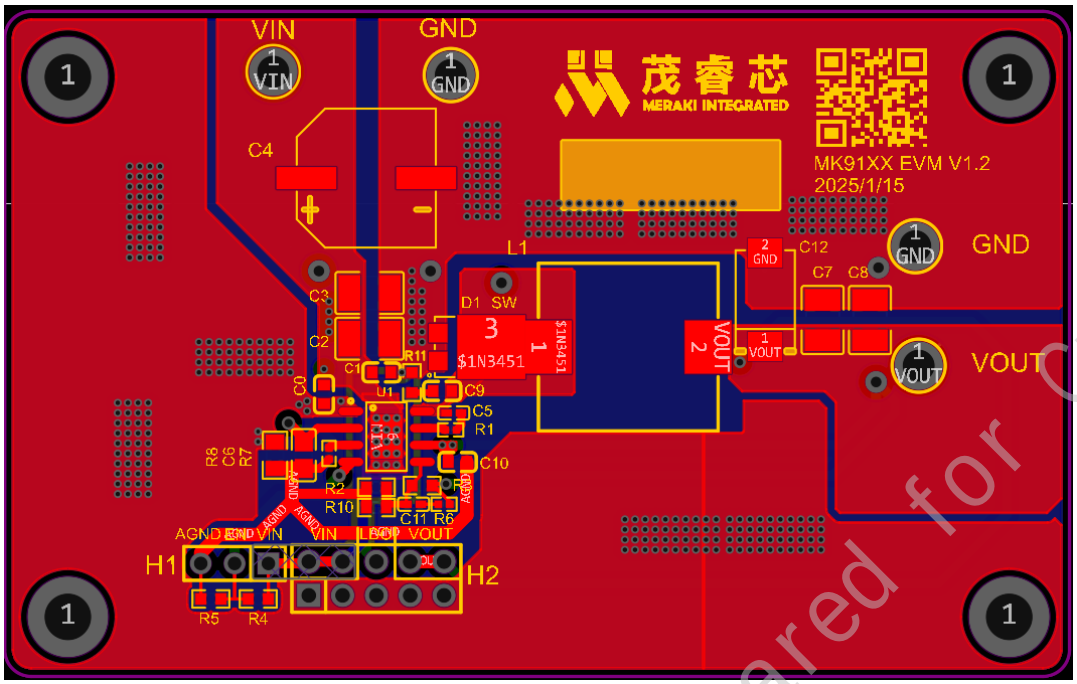


Figure 34. Evkit Layout (Tope Layer)

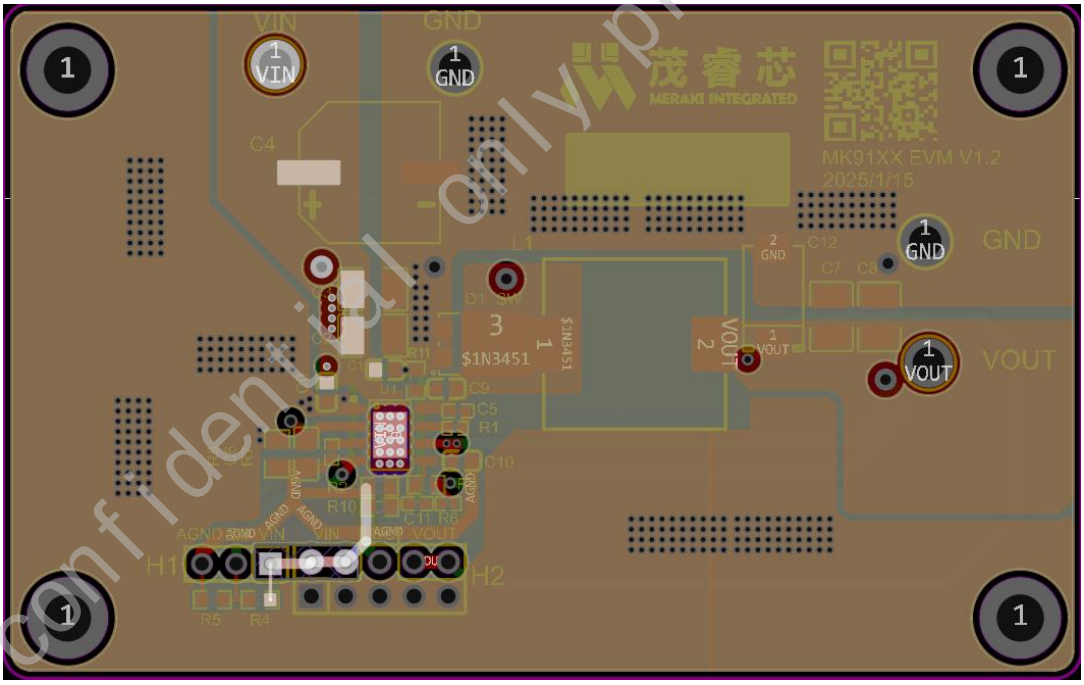


Figure 35. Evkit Layout (Inter1 Layer)

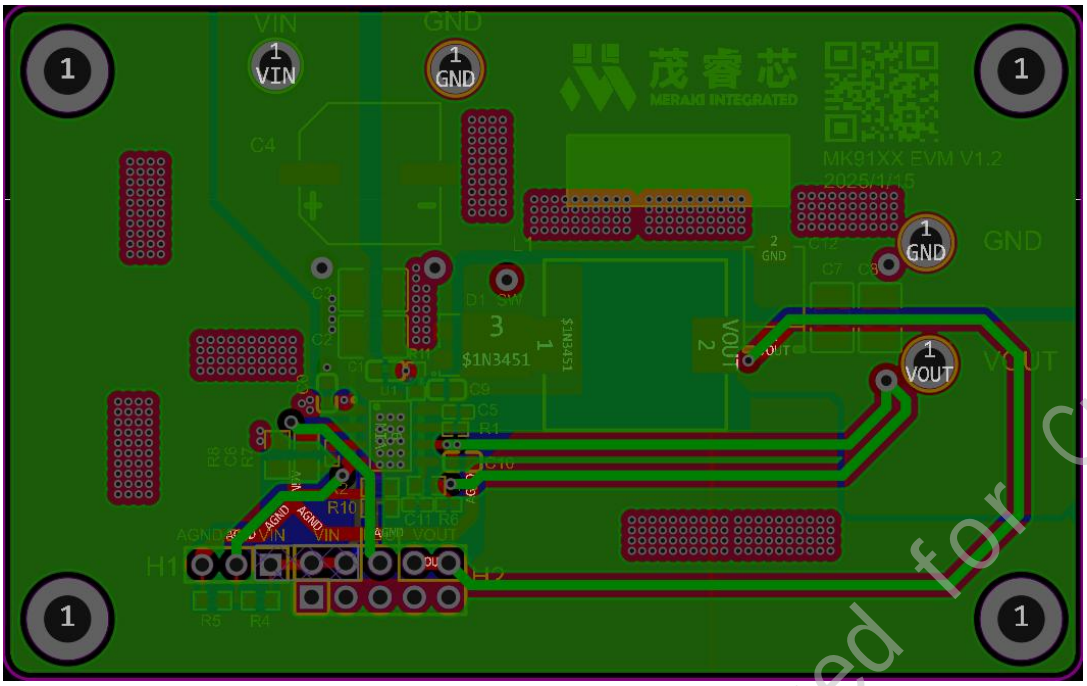


Figure 36. Evkit Layout (Inter2 Layer)

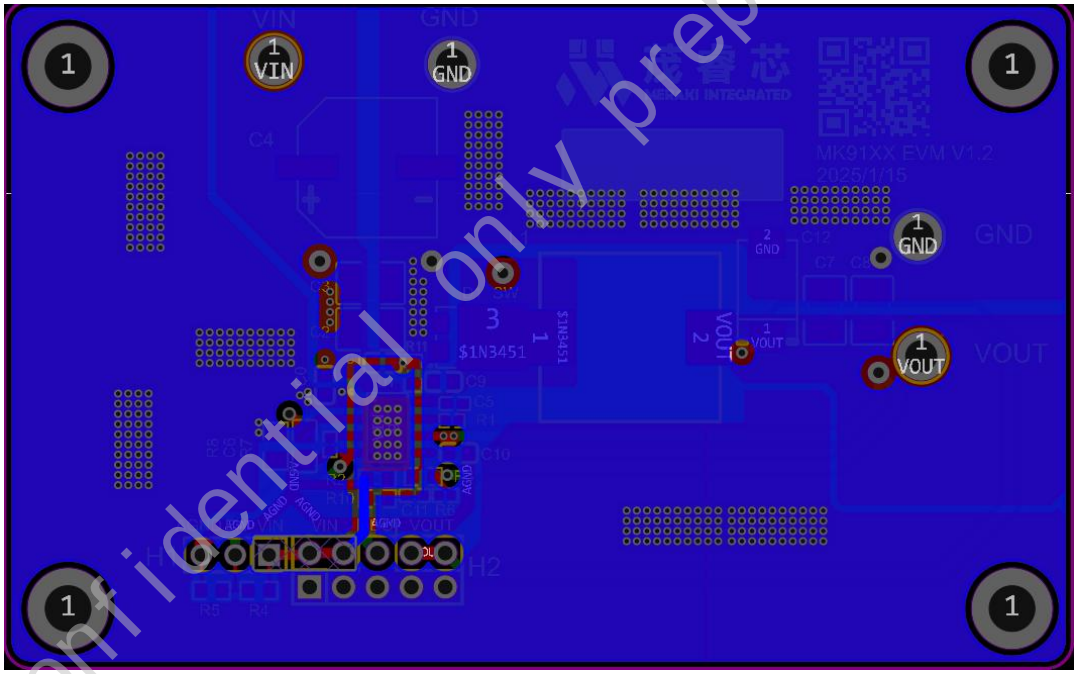


Figure 37. Evkit Layout (Bottom Layer)

12. Device and Documentation Support

12.1 Device Support

12.2 Documentation Support

12.3 Receiving Notification of Documentation Updates

12.4 Support Resources

12.5 Trademarks

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Meraki Integrated recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13. Mechanical, Packaging

13.1 Package Size

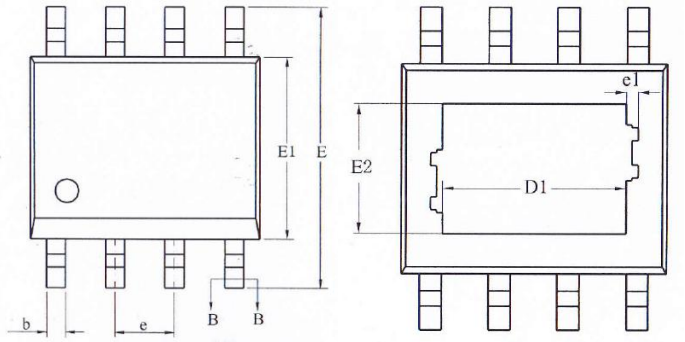


Figure 38. MK9163/5 Top View

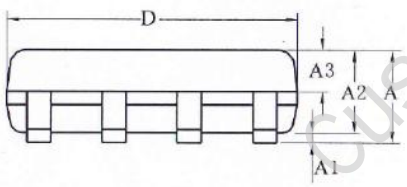


Figure 39. MK9163/5 Side View

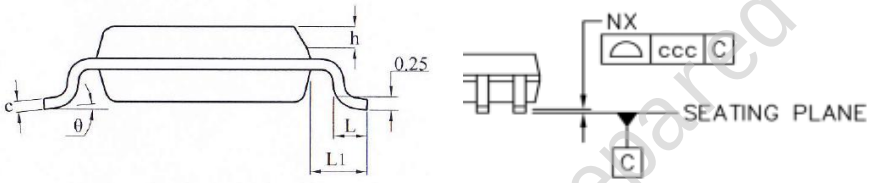


Figure 40. MK9163/5 Side View and Coplanarity

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	1.50	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
b	0.39	-	0.47
c	0.20	-	0.24
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
D1	3.1REF		
E2	2.21REF		
e	1.27(BSC)		
L	0.5	-	0.8
θ	0°	-	8°
Coplanarity (ccc) ⩽ 0.10mm			

13.2 Recommended Land Pattern

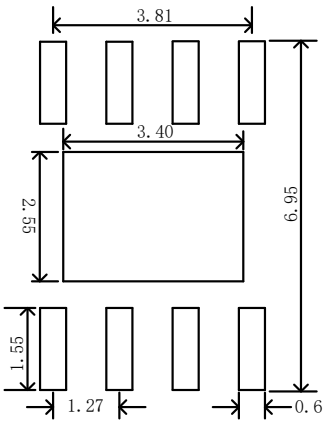


Figure 41. MK9163/5 Recommended Land Pattern (mm)

Notes: (continued):

(1) All linear dimensions are in millimeters.

(2) It is recommended that vias under paste be filled, plugged or tented.

14. Reel and Tape Information

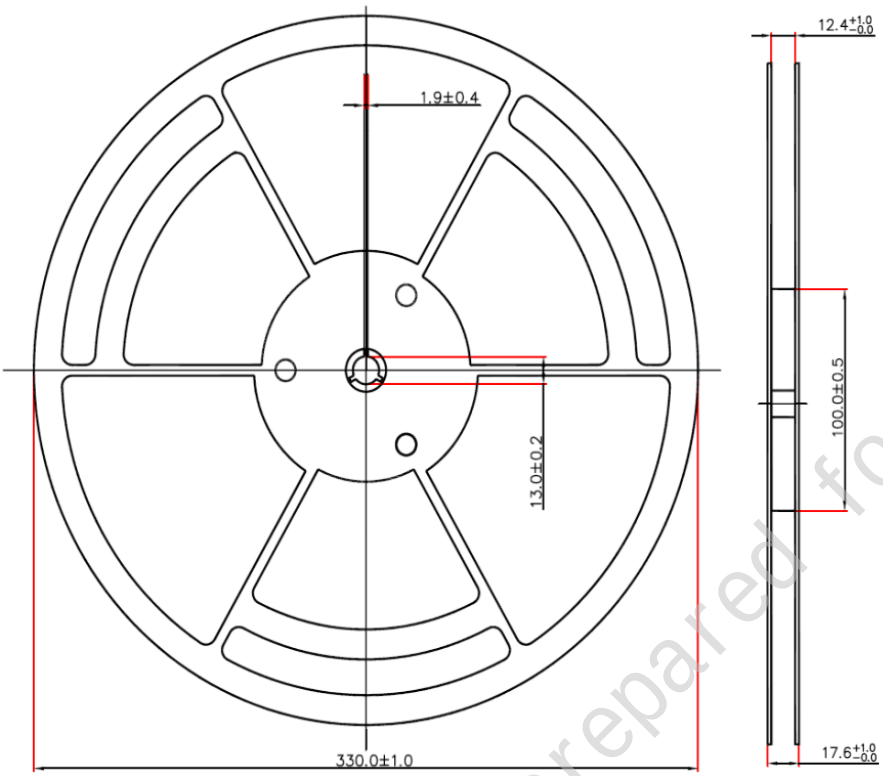
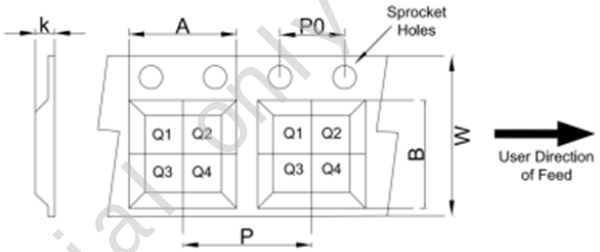


Figure 42. Reel Dimensions

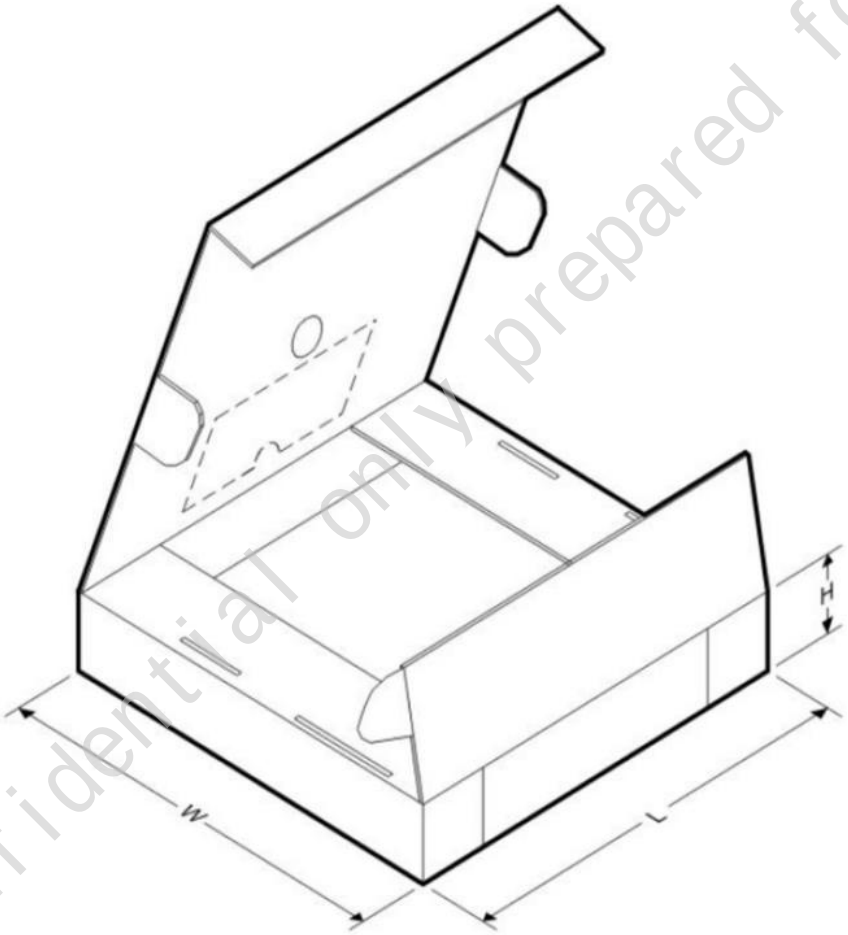


Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MK9163CAD	ESOP-8	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8±0.1	4.0±0.1	12±0.1	Q1
MK9165CAD										

Figure 43. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

15. Tape and Reel Box Dimensions

(Please refer to MRX-DM-QA-05 for detailed rules)



Device	Package Type	Pins	SPQ	Length	Width	Height
			(pcs)	(mm)	(mm)	(mm)
MK9163CAD	ESOP-8	8	8000	360	360	65
MK9165CAD						

Figure 44. Box Dimensions