3 A Peak, High Voltage, High Frequency High-Side and Low-Side Driver with Enable and Interlock

1. Description

The MD18208 high-frequency gate driver integrates a 120-V bootstrap diode and is designed to drive both high-side and low-side N-Channel MOSFETs with maximum control flexibility through independent inputs.

The inputs can handle -10V to 20V DC, which increases robustness against ringing from gate transformers and/or parasitic inductance in long routing traces. The device also has input interlock functionality, which shuts off both outputs when the two input signals overlap.

The high-side driver is protected from negative spikes at HS pin down to -18V, caused by parasitic inductance and stray capacitance.

With 16ns rising and falling propagation delay, the driver enables systems to operate at high frequencies with minimal delay-matching variations.

The MD18208 is available in SOP-8, DFN 3X3-10, and DFN 4X4-8 packages.

2. Typical Applications

- Power Supplies for Telecom, Datacom, and 48V to 72V Battery Powered Systems
- Half-Bridge Applications and Full-Bridge Converters
- Push-Pull Converters
- High Voltage Synchronous Buck Converters
- Two-Switch Forward Converters
- Active Clamp Forward Converters
- Class-D Audio Amplifiers

3. Features

- Drives Both High-Side and Low-Side N-Channel MOSFETs with Independent Inputs
- Operating Switching Frequency up to 1MHz
- Bootstrap Supply Voltage up to 120V DC
- Enable (exclusive to DFN3x3-10 package parts) and interlock functions
- 3A Source and Sink Output Peak Currents
- 11-ns Rise and 8-ns Fall Time with 1000-pF Load
- Input Pins Can Tolerate -10V to +20V, and are Independent of Supply Voltage Range
- TTL Compatible Inputs
- 5.5V to 17V VDD Operating Range, 20V ABS MAX
- Fast Propagation Delay Times
- Excellent Propagation Delay Matching (1ns Typical)
- Symmetrical Undervoltage Lockout for High-Side and Low-Side Drivers

4. Typical Application

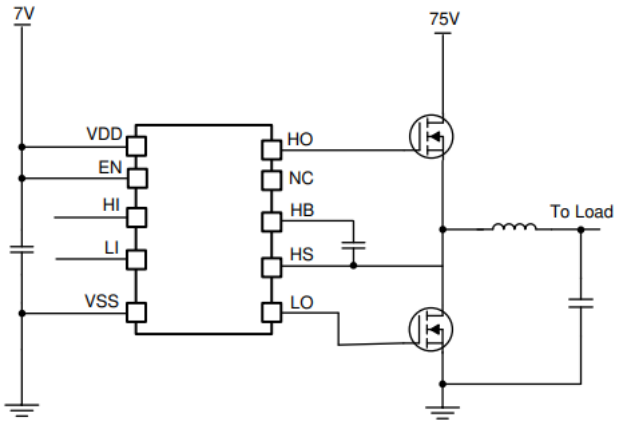

Figure 1. Typical Application Diagram

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5. Order Information

Encapsulation encoding

A2A3: Encapsulated form code;

A1: 1. For products containing MOS or GAN encapsulation, the model representing MOS or GAN;

2. For products that do not contain MOS or GAN, in principle, the letter "X" is uniformly used; In special cases, it can be used as the identification of special specifications of products, using A/B/C... and other letters instead;

Order Code	Package	PINS	SPQ (pcs)
MD18208XDK	DFN 3X3	10	3000
MD18208XDA	DFN 4X4	8	3000
MD18208XAB	SOP	8	4000

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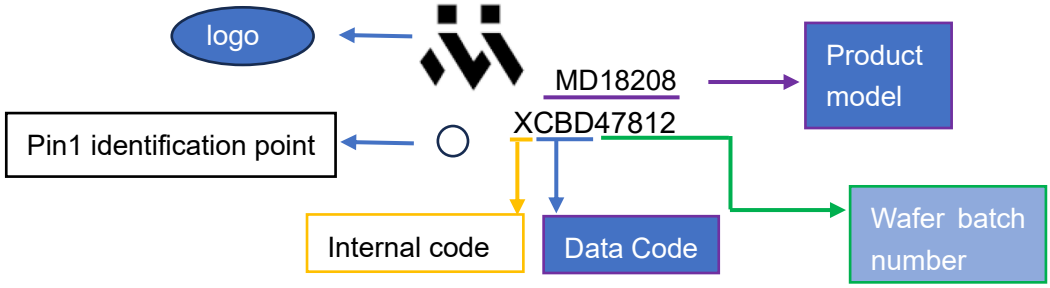
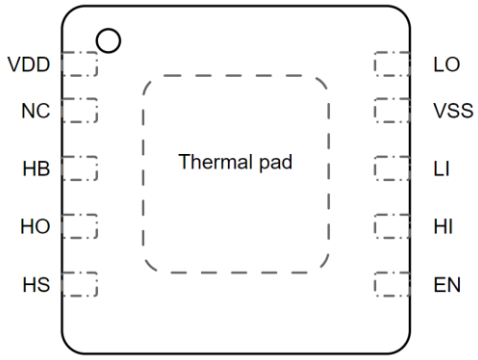
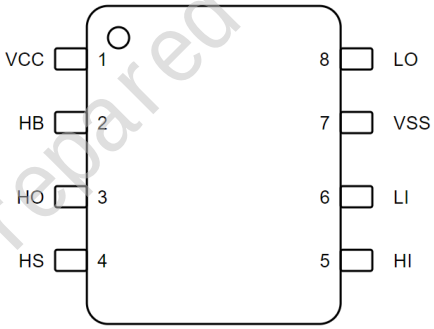
6. Package Reference and PIN Functions



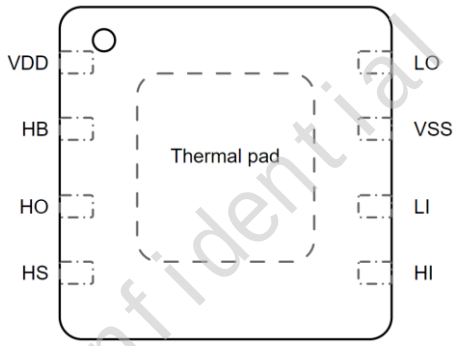
(please refer to MRX-DM-SCM-04 for detailed rules)



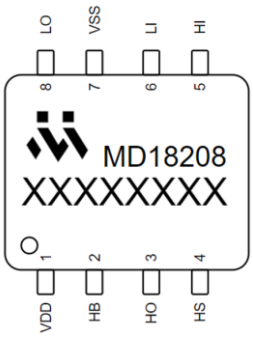
DFN 3x3-10 (top view)



SOP-8 (top view)



DFN 4x4-8(Top View)



MD18208 top marking data code

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PIN			Name	Description
SOP-8	DEN4x4-8	DFN3x3-10		
1	1	1	VDD	Positive gate drive supply. Locally decouple to VSS using low ESR/ESL capacitor located as close to the device as possible
		2	NC	Not connected internally
2	2	3	HB	High-side bootstrap supply. Connect to the positive terminal of bootstrap capacitor that should be placed as close to the device as possible.
3	3	4	HO	High-side gate driver output. Connect to the gate of high-side MOSFET with a short, low inductance path
4	4	5	HS	High-side source connection. Connect to the negative terminal of bootstrap capacitor and the source of the high-side N-Channel MOSFET
\	\	6	EN	Enable input. When this pin is pulled high, it will enable the driver. If left floating or pulled low, it will disable the driver. 1nF filter capacitor is recommended for high-noise systems.
5	5	7	HI	High-side input
6	6	8	LI	Low-side input
7	7	9	VSS	Negative supply for the device that is generally grounded. All signals of the device are referenced to this ground
8	8	10	LO	Low-side gate driver output. Connect to the gate of low-side MOSFET with a short, low inductance path

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7. Specifications

7.1 Absolute Maximum Ratings (1)

		MIN	MAX	UNIT
VDD		-0.3	20	V
V_{EN}, V_{HI}, V_{LI}		-10	20	V
V_{LO}	DC	-0.3	VDD+0.3	V
	Pulse ≤ 100ns (2)	-2	VDD+0.3	V
	Pulse ≤ 30ns (2)	-5	VDD+0.3	V
HO-HS	DC	-0.3	VDD+0.3	V
	Pulse ≤ 100ns (2)	-2	VDD+0.3	V
	Pulse ≤ 30ns (2)	-5	VDD+0.3	V
HS-VSS	DC	-5	110	V
	Pulse ≤ 100ns (2)	-18	115	V
HB-VSS		-0.3	120	V
Power dissipation at T_A=25℃ (3)			2.7	W
Junction Temperature		-40	150	℃
Lead Temperature (Solder)			260	℃
Storage Temperature		-65	150	℃

Notes:

(1) Exceeding these ratings may cause permanent damage to the device

(2) Verified at bench characterization

(3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature.

7.2 Recommend Operation Conditions (1)

		MIN	MAX	UNIT
VDD		5.5	17	V
V_{EN}, V_{HI}, V_{LI}		-5	17	V
HS-VSS	DC	-1	105	V
	Pulse ≤ 100ns (2)	-18	110	V
V_{HB}		HS+5.5	HS+17	V
HS slew rate			50	V/ns
Operating Junction Temperature (T_J)		-40	140	℃
Ambient Temperature		-40	125	℃

Notes:

(1) The device is not guaranteed to function outside of its operating conditions.

(2) Verified at bench characterization

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7.3 Thermal Resistance

	$R_{\theta JA}$	$R_{\theta JC\ (TOP)}$	$R_{\theta JC\ (BOTTOM)}$	Unit
DFN 3x3-10	64	75	8	°C/W
DFN 4x4-8	52	49	8	°C/W
SOP-8	116	\	47	°C/W

7.4 ESD Ratings

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±2000	V

Notes:

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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7.5 Electrical Characteristics

VDD=V_{HB}=12V, V_{HS}=VSS=0V, T_A=-40°C to +125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Currents						
VDD quiescent current	I_{VDD}	V_{LI}=V_{HI}=0V, with EN pin		0.2	0.4	mA
		V_{LI}=V_{HI}=0V, no EN pin		0.35		mA
VDD operating current	I_{VDDO}	f=500kHz, C_{LOAD}=0		1.0	2.5	mA
HB total quiescent current	I_{HB}	V_{LI}=V_{HI}=0V		0.2	0.4	mA
HB total operating current	I_{HBO}	f=500kHz, C_{LOAD}=0		1.0	2.5	mA
HB to VSS quiescent current	I_{HBS}	V_{HS}=V_{HB}=110V		1	20	µA
HB to VSS operating current	I_{HBSO}	f=500kHz, C_{LOAD}=0		0.1	1	mA
I_{VDD} when driver is disabled	I_{VDD_DIS}	V_{EN} = 0		11	30	uA
Inputs						
Input voltage rising threshold	V_{ITH}		1.8	2.1	2.4	V
Input voltage falling threshold	V_{ITL}		0.9	1.1	1.3	V
Input voltage hysteresis	V_{ITHYS}			1.0		V
Input pulldown resistance	R_{IN}		100	200	350	kΩ
EN voltage rising threshold	V_{EN_ON}			1.5	1.8	V
EN voltage falling threshold	V_{EN_OFF}		0.9	1.2		V
EN voltage hysteresis	V_{EN_HYS}			0.3		V
EM pulldown resistance	R_{EN}		100	200	350	kΩ
Undervoltage Lockout						
VDD rising threshold	V_{DDR}			4.95	5.4	V
VDD falling threshold	V_{DDF}		4	4.45		
VDD threshold hysteresis	V_{DDHYS}			0.5		V
HB rising threshold	V_{HBR}			3.65	4	V
HB falling threshold	V_{HBF}		2.8	3.25		
HB threshold hysteresis	V_{HBHYS}			0.4		V
Bootstrap Diode						
Low-current forward voltage	V_{FL}	I_{VDD-HB}=100µA		0.65	0.85	V
High-current forward voltage	V_{FH}	I_{VDD-HB}=80mA		1.0	1.2	V
Dynamic resistance, $\Delta V_F/\Delta I$	R_D	I_{VDD-HB}=100mA and 80mA		1.2	2	Ω
LO Gate Driver						
Low-level output voltage	V_{LOL}	I_{LO}=100mA		0.1	0.3	V
High-level output voltage	V_{LOH}	I_{LO}=-100mA, V_{LOH}=VDD-LO		0.18	0.3	V
Peak pull-up current		V_{LO}=0V		3		A
Peak pull-down current		V_{LO}=12V		3		A
HO Gate Driver						
Low-level output voltage	V_{HOL}	I_{HO}=100mA		0.1	0.3	V
High-level output voltage	V_{HOH}	I_{HO}=-100mA, V_{HOH}=HB-HO		0.18	0.3	V

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Peak pull-up current		V_{HO}=0V		3		A
Peak pull-down current		V_{HO}=12V		3		A
Propagation Delays						
LO turn-on propagation delay	T_{DLR}	LI rising to LO rising		16	30	ns
HO turn-on propagation delay	T_{DHR}	HI rising to HO rising		16	30	ns
LO turn-off propagation delay	T_{DLF}	LI falling to LO falling		16	30	ns
HO turn-off propagation delay	T_{DHF}	HI falling to HO falling		16	30	ns
Delay Matching						
From HO OFF to LO ON	T_{MON}			1	7	ns
From LO OFF to HO ON	T_{MOFF}			1	7	ns
En Propagation Delays						
EN turn-on propagation delay	T_{EN_ON}	EN rising to HO or LO rising		18	40	us
EN turn-off propagation delay	T_{EN_OFF}	EN falling to HO or LO falling		1.75	4	us
Output Rise and Fall Time						
LO, HO rise time		C_{LOAD}=1000pF		11		ns
LO, HO fall time		C_{LOAD}=1000pF		8		ns
LO, HO rise time		C_{LOAD}=100nF		0.45	0.8	us
LO, HO fall time		C_{LOAD}=100nF		0.4	0.7	us
Miscellaneous						
Minimum input pulse width that changes the output				10	40	ns

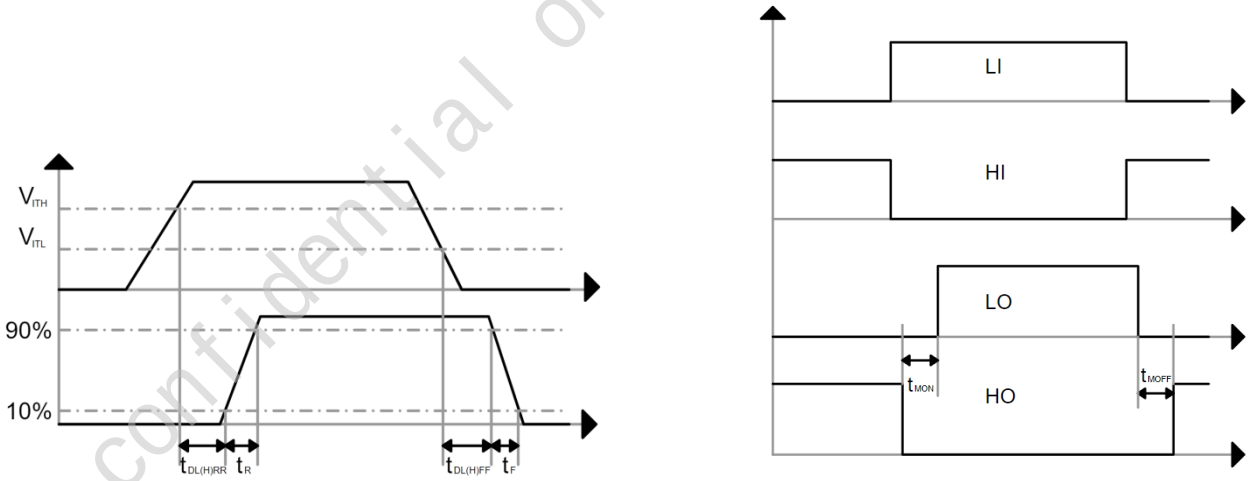

Figure 2. Timing Diagram

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7.6 Typical Characteristics

VDD=VHB=VEN=12V, VHS=VSS=0V, T_A=25℃, unless otherwise noted.

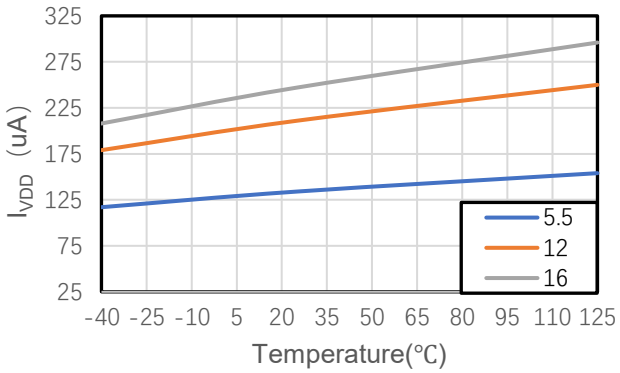

Figure 3. VDD Quiescent Current

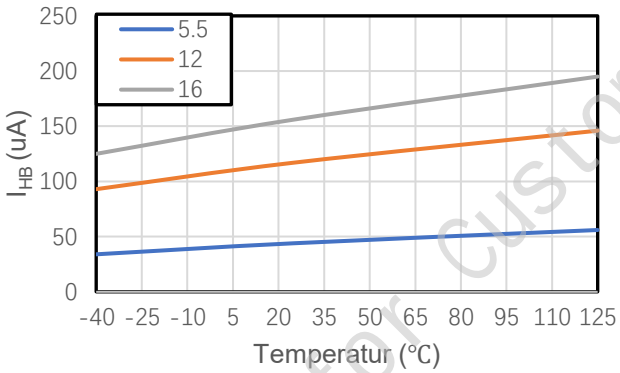

Figure 4. HB Quiescent Current

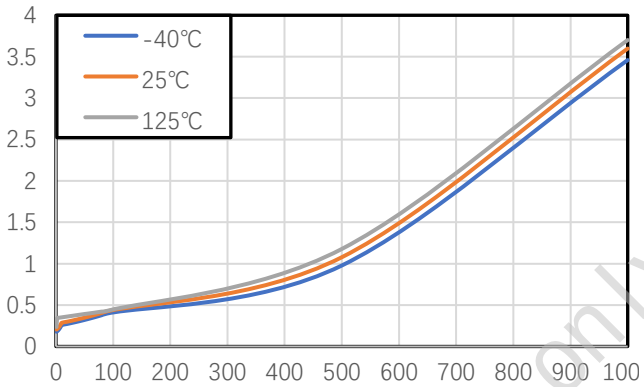

Figure 5. VDD Operating Current

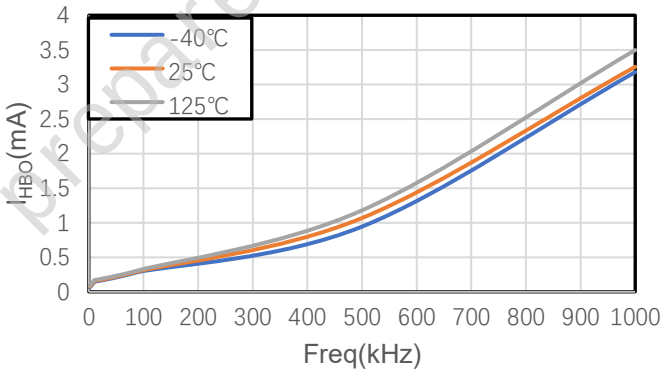

Figure 6. HB Operating Current

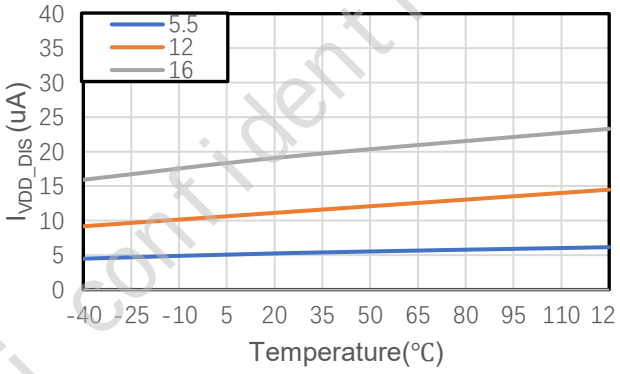

Figure 7. VDD Current When Disabled (VEN=0)

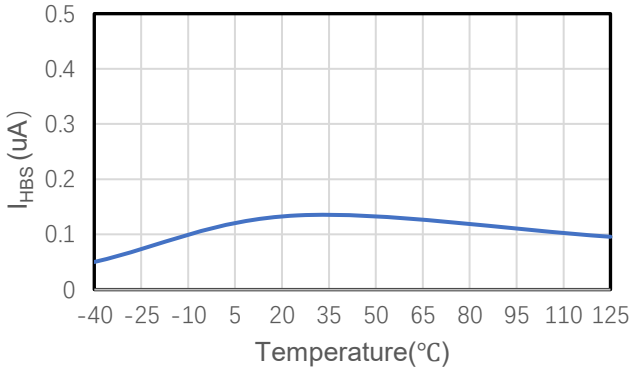

Figure 8. HS to VSS Quiescent Current (HB=HS=110V)

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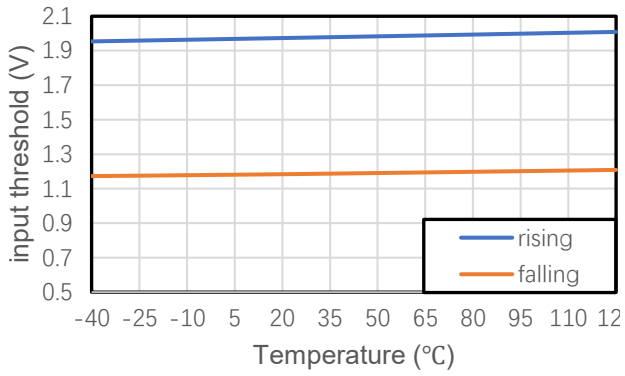

Figure 9. Input Rising and Falling Threshold

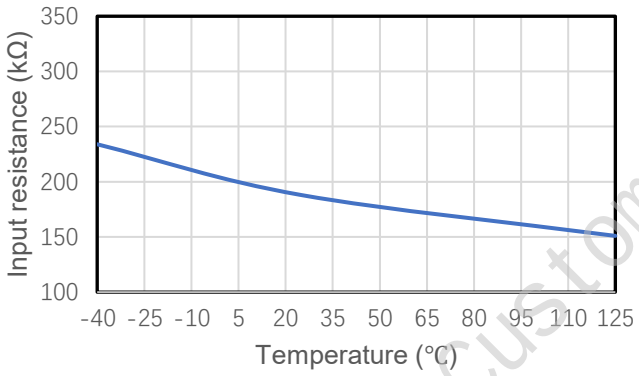

Figure 10. Input Pull-down Resistance

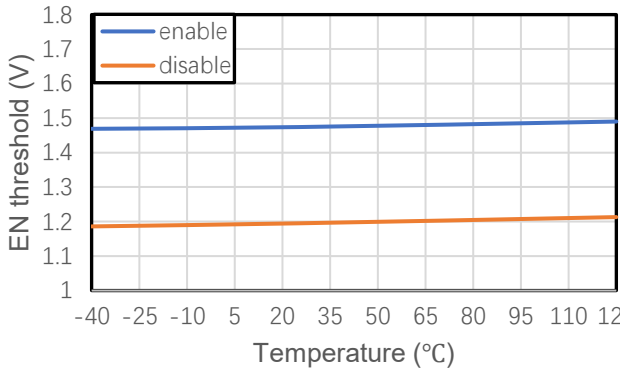

Figure 11. Enable and Disable threshold

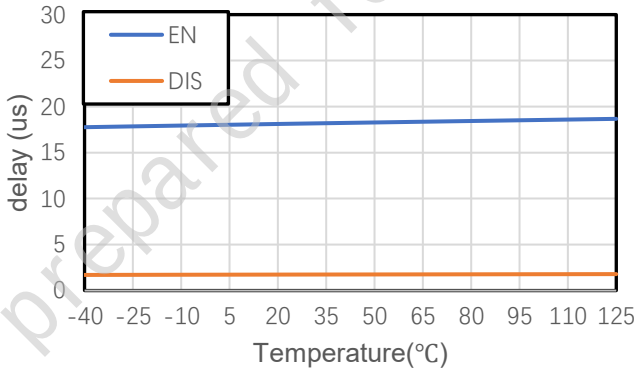

Figure 12. Enable and Disable Delay

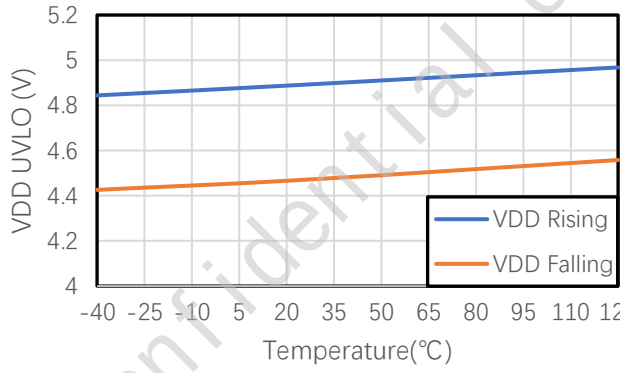

Figure 13. VDD UVLO Threshold

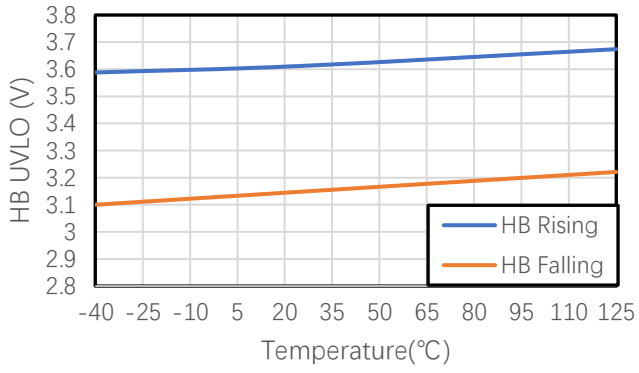

Figure 14. HB UVLO Threshold

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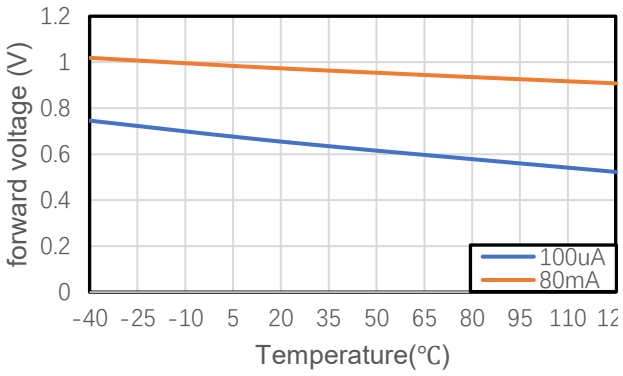

Figure 15. Boot Diode Forward Voltage

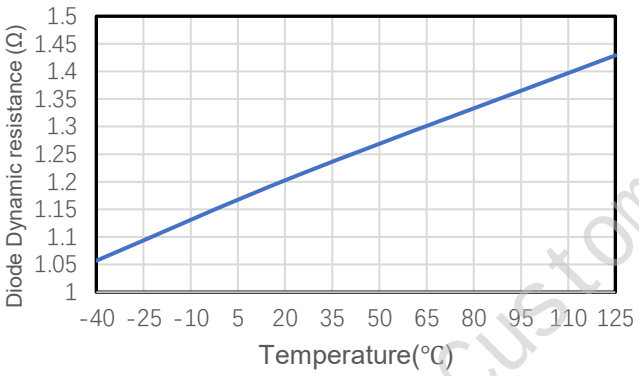

Figure 16. Boot Diode Dynamic Resistance

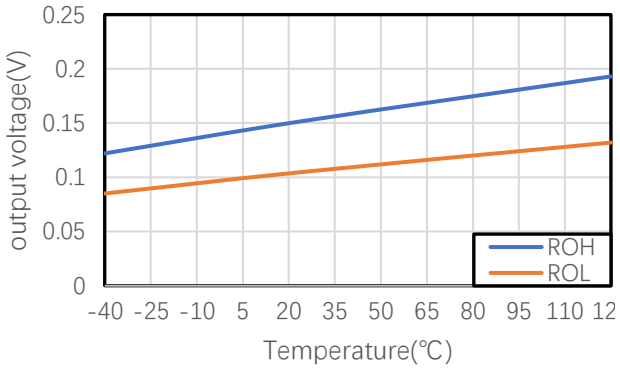

Figure 17. HO output voltage

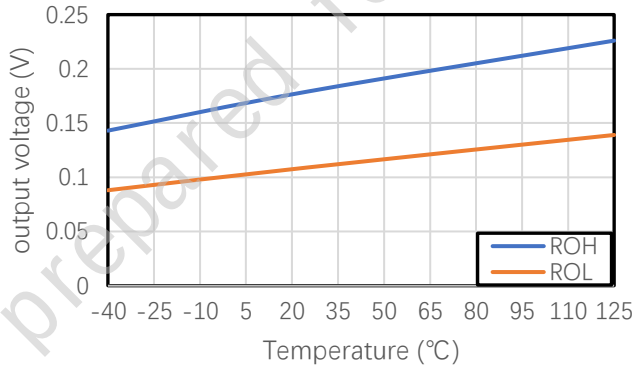

Figure 18. LO output Voltage

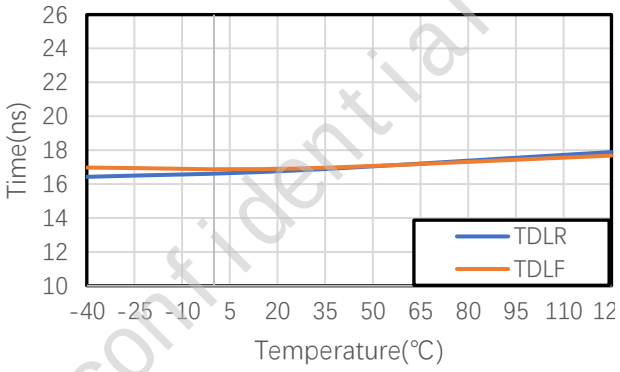

Figure 19. LO Propagation Delay

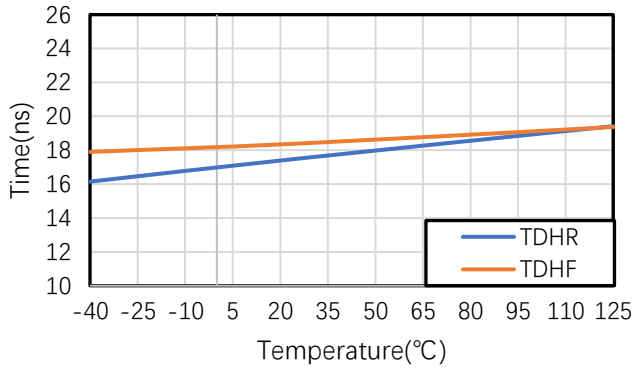

Figure 20. HO Propagation Delay

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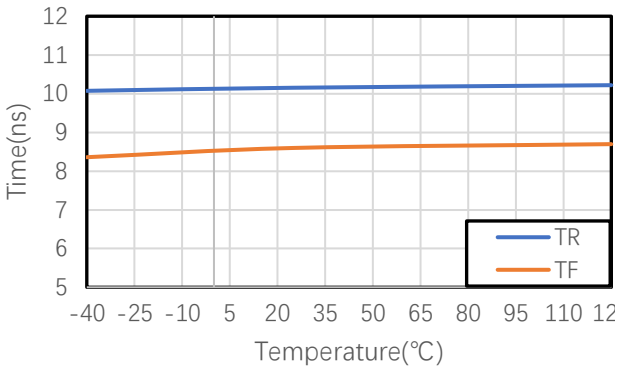

Figure 21. HO rise and fall time

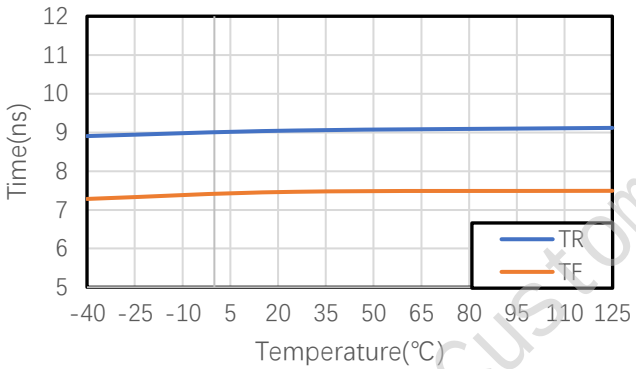

Figure 22. LO rise and fall time

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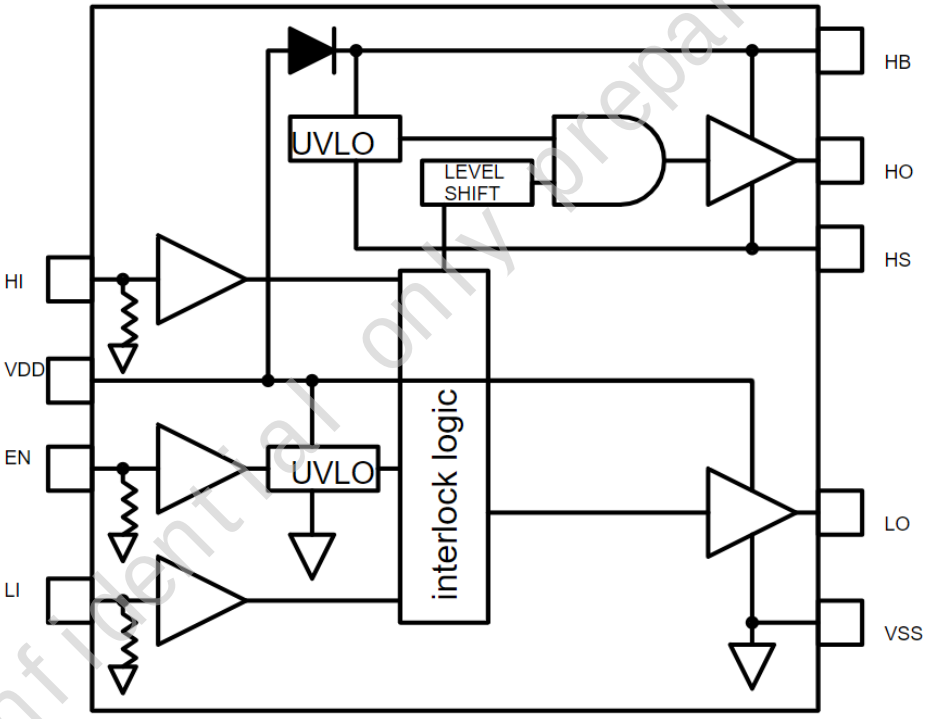
8. Operation

8.1 Overview

The MD18208 is a gate driver designed to drive both high-side and the low-side N-Channel MOSFETs in half-bridge, full-bridge, synchronous-buck, synchronous-boost, push-pull, two-switch forward, and active clamp forward converters. The high-side and low-side channels each feature independent inputs, enabling maximum flexibility for input control signals. These inputs can handle a DC voltage range of -10V to 20V, enhancing robustness against voltage transients from gate transformers and/or parasitic inductance in long routing traces within the application. The high side driver can operate with HS voltage up to 110V relative to GND and is protected against negative spikes down to -18V at the HS pin —these spikes are typically caused by parasitic inductance and stray capacitance. A 120V bootstrap diode for the high-side driver's bias supply is integrated internally in the MD18208. An EN pin is provided (exclusive to parts in the DFN3x3-10 package) to enable or disable the driver. Additionally, the driver incorporates input interlock functionality, which shuts off both the outputs if the two inputs overlap.

8.2 Block Diagram



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8.3 Functional Modes

MD18208 operates in normal mode and UVLO mode. In the normal mode, the output state depends on states of the input pins. See below tables:

Table1. DFN3x3-10 packages logic

EN PIN	HI PIN	LI PIN	HO PIN	LO PIN
X	floating	floating	L	L
L/floating	X	X	L	L
H	L	L	L	L
H	H	L	H	L
H	L	H	L	H
H	H	H	L	L

Table 2. DFN4x4-8 and SOP-8 packages logic

HI PIN	LI PIN	HO PIN	LO PIN
L	L	L	L
H	L	H	L
L	H	L	H
H	H	L	L

Notes:

1) HO is measured with respect to HS

2) LO is measured with respect to VSS

3) X means high or low

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8.4 Input Stages and Interlock

The two inputs (HI and LI ports) are independent, except that both outputs will be pulled low quickly if both inputs are high or their signals overlap. The MD18208 incorporates an interlock function, ensuring only one output is active at a time to drive the MOSFET—preventing shoot-through. The input pins of MD18208 use TTL-compatible input-threshold logic. The input voltage range is independent of the VCC supply voltage. With a typical high threshold (V_{ITH}) of 2.2V, a typical low threshold (V_{ITL}) of 1.2V, both with minimal variation over temperature, and a wide hysteresis (V_{ITHYS}) of 1V, the MD18208 delivers strong noise immunity and stable operation. This makes it easily driven by PWM control signals from 3.3V and 5V digital power-controller devices. The inputs have internal pull-down resistors with a typical value of 200kΩ. Furthermore, if the inputs are left floating, both outputs remain held low.

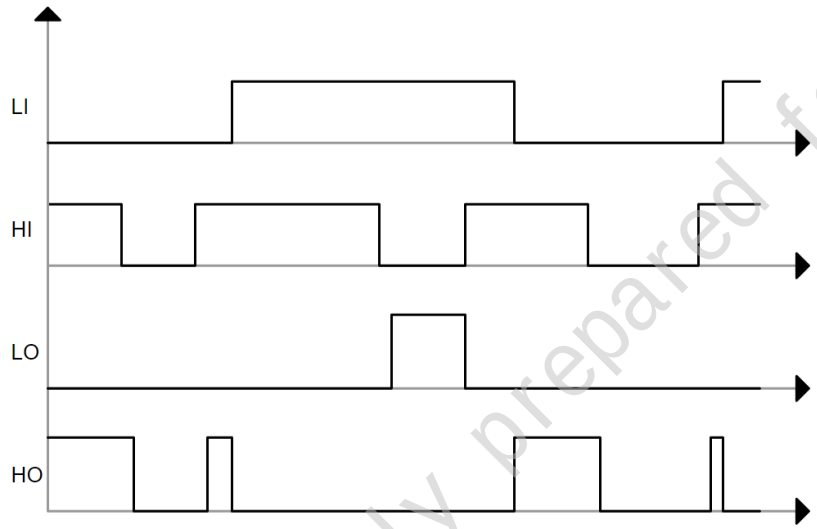

Figure 23. Interlock logic diagram

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8.5 Enable Function

MD18208 includes an Enable (EN) pin, which is exclusive to the DFN 3x3-10 package. The outputs will only be activated if the EN voltage exceeds the threshold voltage (V_{EN_ON}). The outputs will be held low if the EN voltage is floating or falls below the threshold voltage (V_{EN_OFF}). The EN pin features internal pull-down resistors with a typical value of 200kΩ. It is recommended to connect it to the VDD pin if the EN pin is not used. For pull-up resistor configurations, a strong pull-up structure is recommended: with a 12V power supply, a 10kΩ pull-up is suggested. To enhance noise immunity, a small capacitor of 1nF should be connected between the EN pin and VSS pin, and this capacitor must be placed as close to the MD18208 as possible. The EN pin can be connected to the output pin of an analog or a digital controller to enable or disable the driver. Built-in hysteresis for the EN pin prevents nuisance tripping or chattering of the driver's outputs.

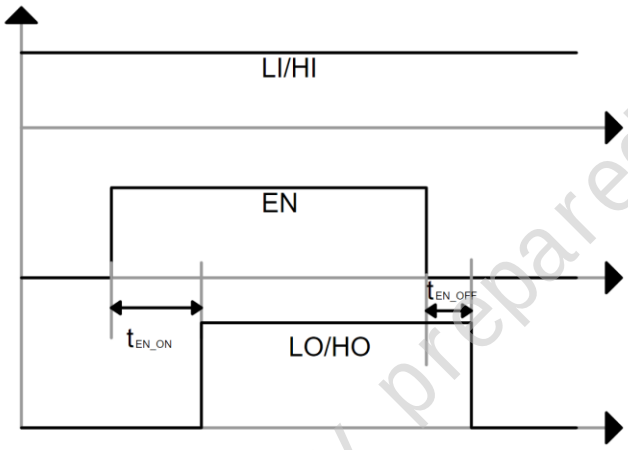

Figure 24. Enable and Disable Logic

8.6 Output Stages

The output stages serve as the interface to the power MOSFETs. Both outputs feature low resistance and high peak current capability, enabling efficient switching of the power MOSFETs. The low side output stage is referenced between VDD to VSS, while the high side output stage is referenced between HB to HS.

MD18208 provides excellent output negative voltage handling capability, attributed to its high peak current driving capability and ESD performance of 2kV HBM and 2kV CDM.

8.7 Boot Diode

The boot diode is connected between the VDD pin to HB pin, and is used to charge the boot capacitor connected between HB pin to HS pin. When the HS pin transitions to ground, current from VDD charges the boot capacitor until HS rises. The boot diode provides fast recovery time, low equivalent resistance, and appropriate voltage rating to ensure reliable operation.

8.8 Undervoltage Lockout (UVLO)

The supplies for the high-side (HB to HS) and low-side (VDD to VSS) are monitored. When the VDD voltage falls below the specified threshold, the VDD UVLO disables low-side driver and send the signal by level shift circuit to disable the high-side driver. When the HB-to-HS voltage falls below the specified threshold, the HB UVLO disables only the high-side driver.

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8.9 Level Shifter

The level shift circuit interfaces the high-side input to the high-side driver stage, which is referenced to the switch node (HS). This circuit enables control of the HO output (referenced to the HS pin) and provides excellent delay matching with the low-side driver.

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9. Application and Implementation

9.1 Typical Applications

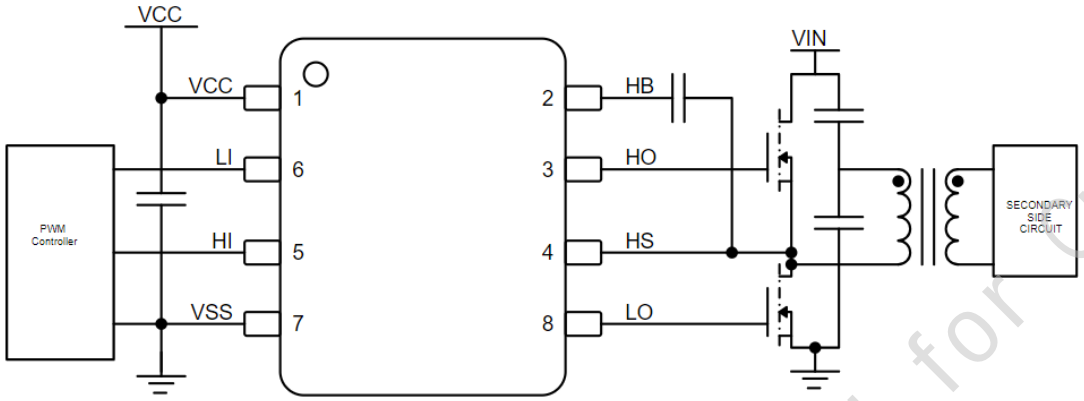

Figure 25. MD18208 Typical Application: Half Bridge

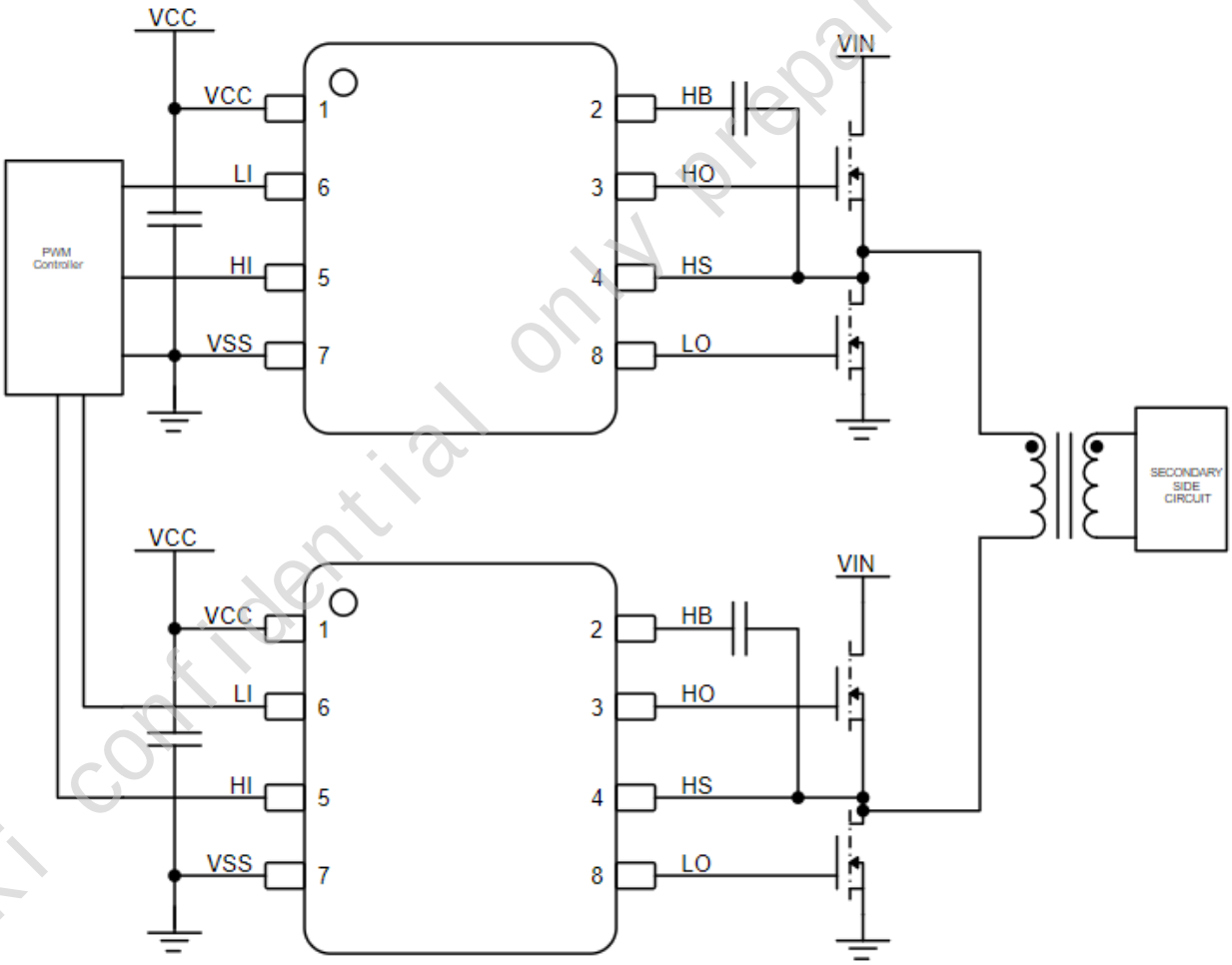

Figure 26. MD18208 Typical Application: Full Bridge

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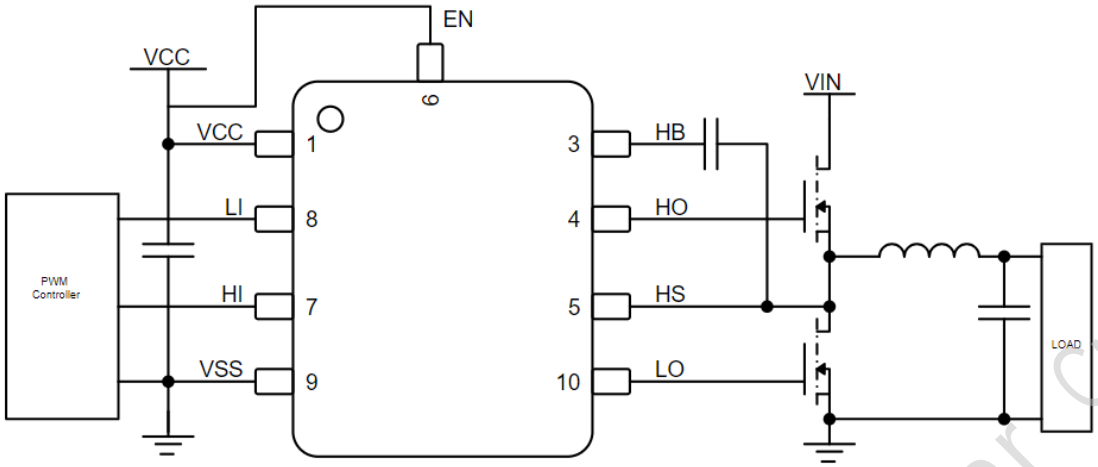

Figure 27. MD18208 Typical Application: Buck

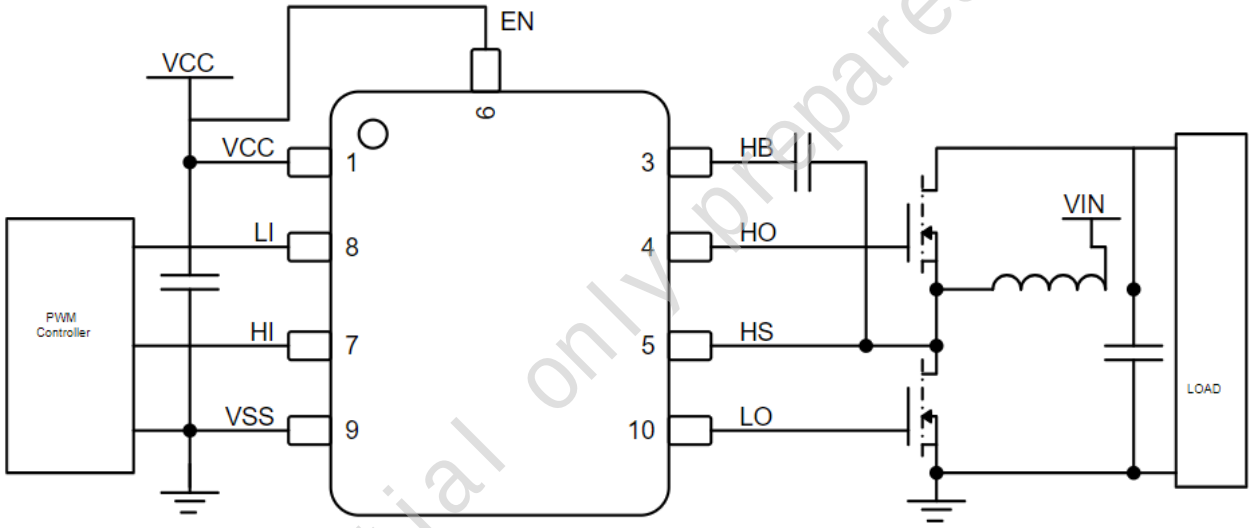

Figure 28. MD18208 Typical Application: Boost

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9.2 Design Procedure

9.2.1 Input Threshold Type

The MD18208 features an input maximum voltage range from -10V to 20V and can be directly interfaced with gate drive transformers. Its threshold voltage levels are independent of the VDD supply voltage, enabling compatibility with logic-level input signals from MCU, DSP as well as analog controllers.
For system applications where there is a long trace from the PWM controller to the driver, it is recommended to add an RC filter near the HI and LI pins.

9.2.2 Supply Voltage

The supply voltage applied to the driver's VDD pin must never exceed the absolute maximum rating. Higher voltages can reduce the conduction loss of MOSFET but will increase switching loss.
The selection of HB-HS and VDD-VSS capacitors depends on the switching frequency and Cgs of MOSFET. Typically, an 100nF(50V) capacitor is used for HB-HS, while VDD-VSS configurations use a 10uF(50V) capacitor in parallel with a 100nF(50V) capacitor. The parallel capacitor serves a decoupling function.

9.2.3 Peak Source and Sink Currents

To minimize switching power losses, MOSFETs should switch on and off as quickly as possible. The gate driver must be able to provide the required peak current to achieve the target switching speeds with the selected power MOSFET.
In system applications, adding a resistor (e.g., 1Ω or 2.2Ω) between the MOSFET gate and the LO/HO pins can control switching speed. Faster turn-on speeds increase MOSFET drain-source stress but reduce switching losses.

9.2.4 Propagation Delay

The gate driver's propagation delay depends on the switching frequency and Cgs of MOSFET. The MD18208 ensures minimal pulse distortion and supports operation at very high frequencies.
When using the MD18208 as a driver in Boost, Buck, or synchronous rectification topologies, the PWM controller must reserve sufficient deadtime between HI and LI signals.

9.2.5 Power Dissipation

The power dissipation of MD18208 consists of two portions as below:
$P_{DISS} = P_{DC} + P_{SW}$
The DC portion of the power dissipation is:
$P_{DC} = I_Q * VDD$
Where IQ is the quiescent current for MD18208. This current is consumed by internal circuits such as the input stage, reference voltage, level shift circuits, and UVLO circuit, excluding current associated with switching internal devices during driver output state changes.
The switching portion of the power dissipation depends on:
(1) Switching frequency f_{SW}
(2) MOSFET gate charge QG
(3) Supply voltage VDD
$P_{SW} = QG * VDD * f_{SW}$

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10. Layout

10.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

(1) Locate the driver close to the MOSFETs.

(2) Locate the VDD-VSS and HB-HS capacitors close to the driver.

(3) Connect the VSS pin to thermal pad and use the thermal pad as GND. The GND trace from MD18208 should go directly to the source of the low side MOSFET but not be in the high current path of MOSFET source current.

(4) Apply the same rules for HS as for GND for the high-side MOSFET.

(5) For systems using multiple drivers, the decoupling capacitors need to be located at VDD-VSS for each driver.

(6) Avoid routing VDD, LI, HI trace close to LO, HS and HO signals, or any other high dV/dT traces that can induce significant noise into the high impedance leads.

(7) Use wide trace for LO and HO to decrease the influence of switching ringing made by parasitic inductance.

(8) If the driver outputs or SW node must be routed from one layer to another, use at least two vias.

(9) For GND, the number of vias must be a consideration of the thermal pad requirements as well as minimizing parasitic inductance.

10.2 Layout Example

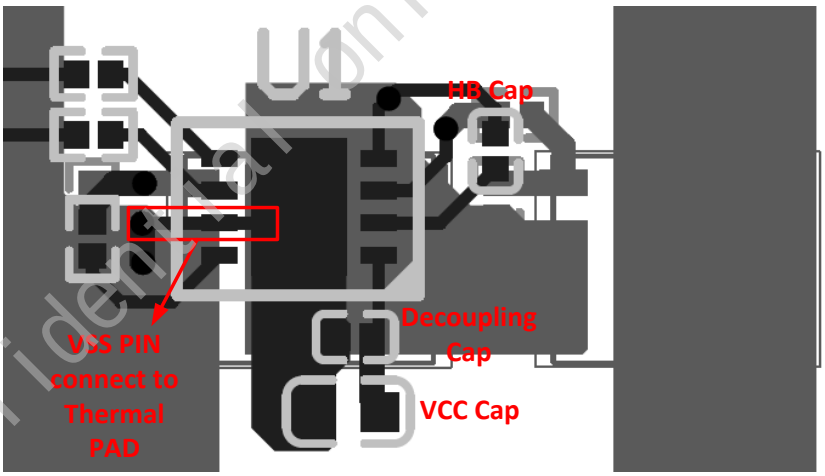

Figure 29. Layout Example

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11. Tape and Reel Information

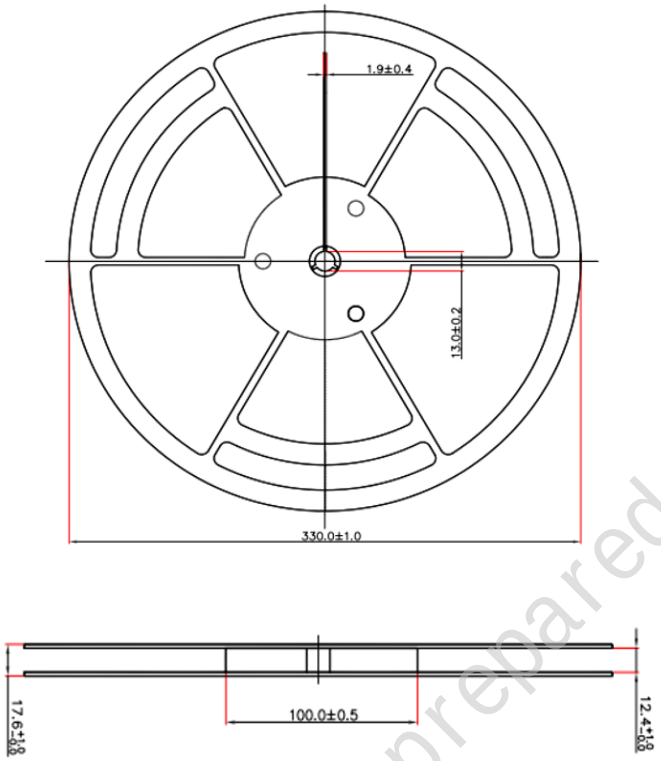
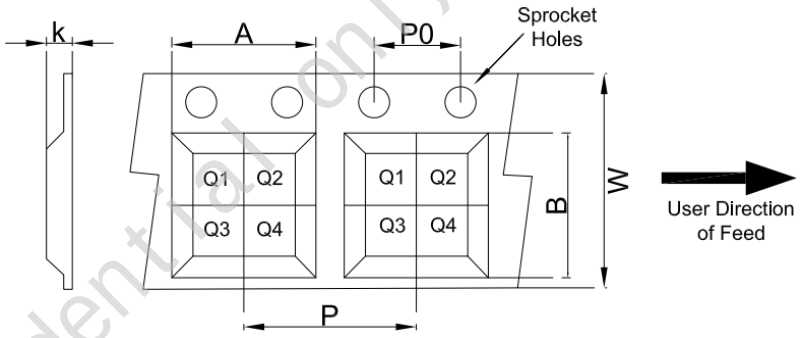


Figure 30. Reel Dimensions



Device	Package Type	Pins	SPQ (pcs)	A (mm)	B (mm)	K (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant
MD18208XDA	DFN 4x4	8	3000	4.3±0.1	4.3±0.1	1.1±0.1	8.0±0.1	4.0±0.1	12.0±0.3	Q2
MD18208XAB	SOP	8	4000	6.5±0.1	5.4±0.1	2.0±0.1	8.0±0.1	4.0±0.1	12.0±0.1	Q1
MD18208XDK	DFN 3x3	10	3000	3.3±0.1	3.3±0.1	1.1±0.1	8.0±0.1	4.0±0.1	12.0±0.3	Q2

Figure 31. Tape Dimensions and Quadrant Assignments for PIN 1 Orientation in Tape

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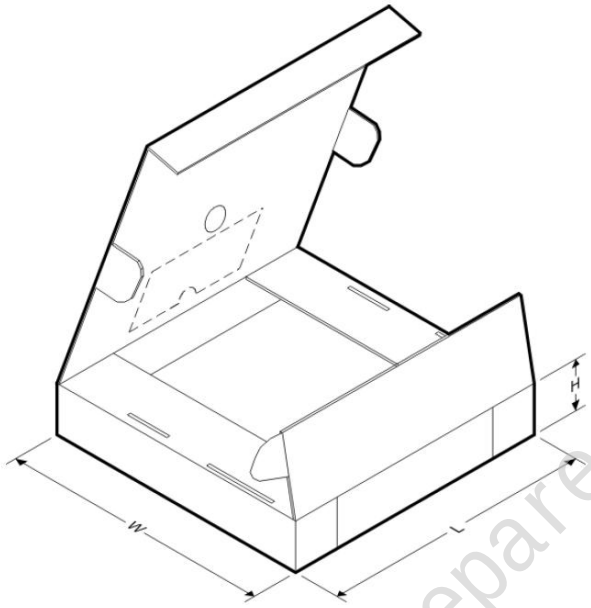
12. Tape and Reel Box Dimensions



Device	Package Type	Pins	SPQ (pcs)	Length (mm)	Width (mm)	Height (mm)
MD18208XDA	DFN 4x4	8	3000	360	360	65
MD18208XAB	SOP	8	8000	360	360	65
MD18208XDK	DFN 3x3	10	3000	360	360	65

Figure 32. Box Dimensions

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13. Mechanical Data and Land Pattern Data

13.1 DFN 4x4-8

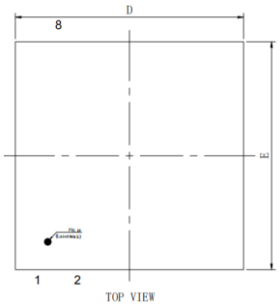

Figure 33. DFN 4x4-8 Top View

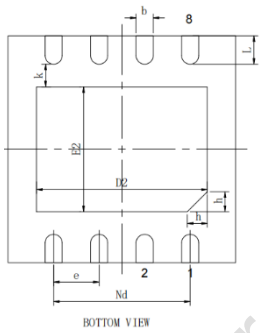

Figure 34. DFN 4x4-8 Bottom View

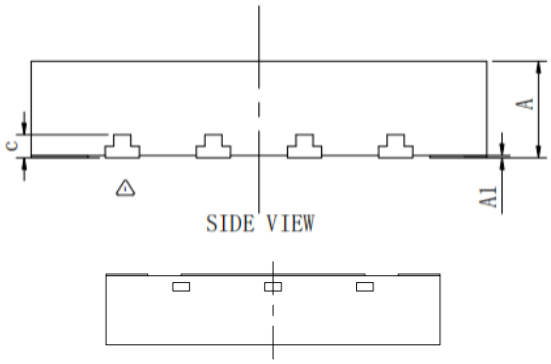

Figure 35. DFN 4x4-8 Side View

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
c		0.203REF	
D	3.90	4.00	4.10
D2	2.90	3.00	3.10
e		0.80BSC	
Nd		2.40BSC	
E	3.90	4.00	4.10
E2	2.10	2.20	2.30
K		0.40REF	
L	0.45	0.50	0.55
h	0.30	0.35	0.40

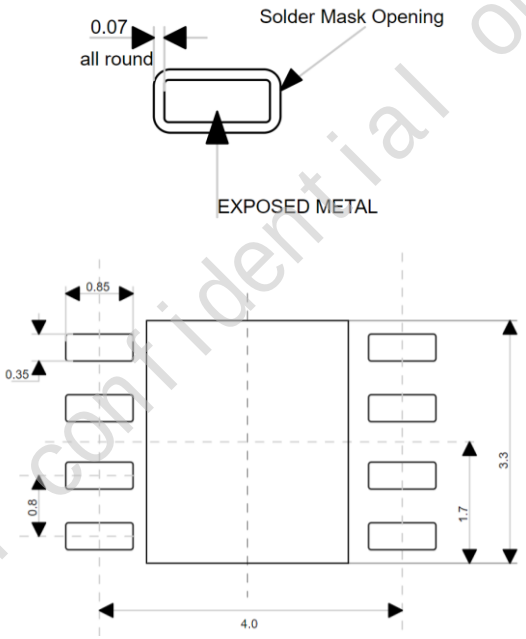

Figure 36. DFN 4X4-8 Land Pattern Data

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13.2 SOP-8

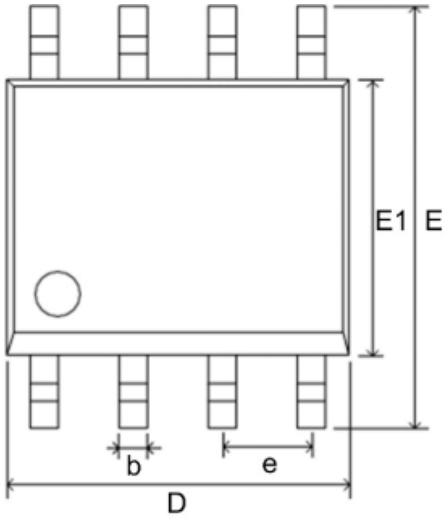

Figure 37. SOP-8 Top View

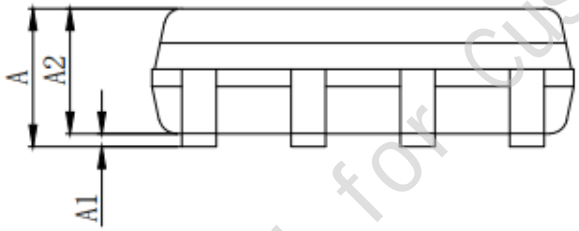

Figure 38. SOP-8 Side View

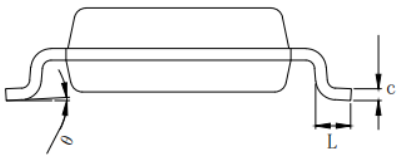

Figure 39. SOP-8 Side View

Symbol	Millimeter		
	MIN	NOM	MAX
A	1.30	1.55	1.75
A1	0.05	-	0.25
A2	1.25	1.40	1.65
b	0.33	-	0.51
c	0.20	-	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27(BSC)		
L	0.4	-	1.27
θ	0°	-	8°

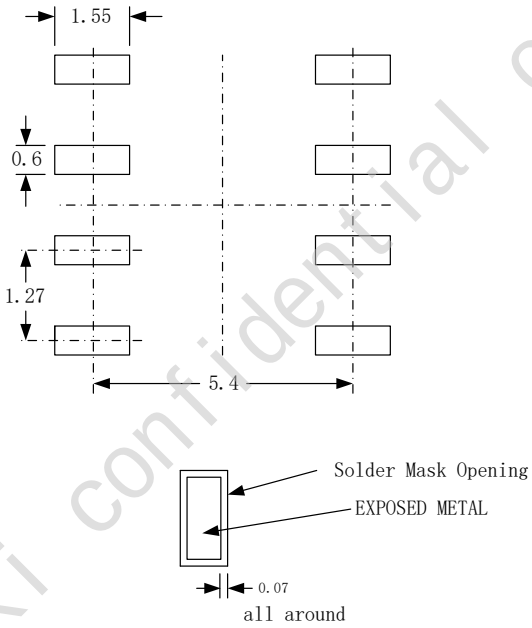

Figure 40. SOP-8 Land Pattern Data

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13.3 DFN 3x3-10

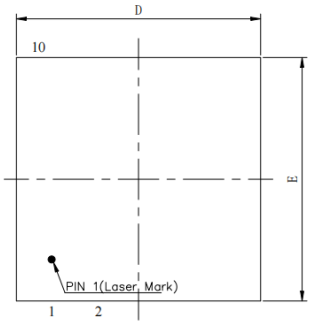

Figure 41. DFN 3x3-10 Top View

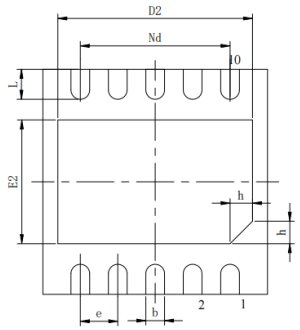

Figure 42. DFN 3x3-10 Bottom View

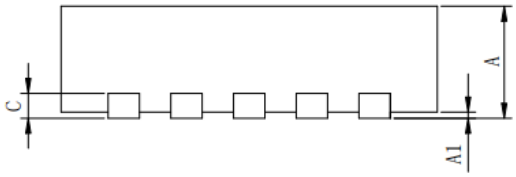

Figure 43. DFN 3x3-10 Side View

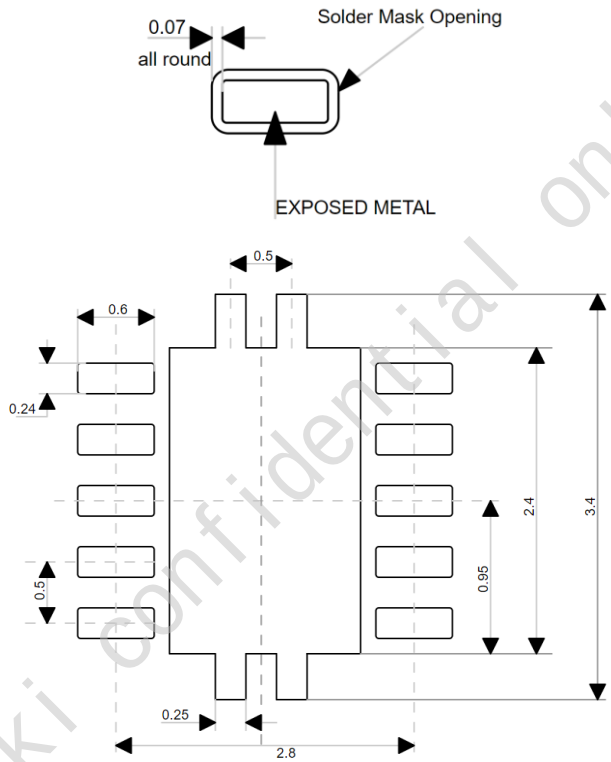

Figure 44. DFN 3x3-10 Land Pattern Data

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c		0.20REF	
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
e		0.50BSC	
Nd		2.00BSC	
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30

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